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High speed ESD protection for RF circuits: Innovative co-designing strategy between FEOL and BEOL devices in advanced technology

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***Abstract*— This paper presents an innovative electrostatic discharge (ESD) protection concept based on the integration of gated diodes within metal-oxide-metal (MOM) capacitors, targeting radio-frequency (RF) applications in advanced CMOS technologies. The proposed ESD capacitor maintains a high quality factor (Q) while providing robust protection against fast transient events, such as those qualified by the charged device model (CDM). The design leverages miniaturized gated diodes and a co-design approach to preserve RF performance without area overhead. Characterization results, including Transmission-Line Pulse (TLP), Very Fast TLP (VF-TLP), and Capacitively Coupled TLP (CC-TLP) tests, demonstrate superior robustness compared to unprotected circuits, with failure currents exceeding 15.1 A in simulations and above 13 A in measurements. The integration of the ESD capacitor into a low-noise amplifier (LNA) operating in the 6–12 GHz range confirms minimal impact on RF parameters such as gain, noise figure, and input matching. These results validate the effectiveness of the proposed solution for high-frequency ESD protection in scaled CMOS technologies.**

***Index Terms*— ESD, RF, Diode, MOM, Capacitor, Q-factor, LNA, TLP, VF-TLP, CC-TLP, CDM.**

I. Introduction

WITH the rapid advancement of microelectronics technologies, circuits have become increasingly sensitive to ESD events due to the continuous scaling down of device dimensions, which increases their vulnerability to external disturbances that directly affect circuit operation [1], [2]. Currently, device dimensions are on the order of tens of nanometers or smaller in the most advanced nodes, making ESD protection design a critical research area [3], [4]. To ensure optimal device functionality, it is essential to maintain the integrity of transistors within the integrated circuit (IC). However, the reduction in the gate oxides thickness and other insulating layers in advanced technologies has increased susceptibility to overvoltage-induced failures, potentially resulting in catastrophic damage caused by ESD events occurring between input, output, or ground pins [5], [6].

This technological scaling has also enabled the reduction of supply voltages for MOS transistors and decreased the voltage tolerance before breakdown, thereby increasing their sensitivity to ESD in RF circuits such as LNA and also power amplifiers (PAs) [7], [8]. Protecting active circuits operating at RF frequencies, particularly in the tens of giga hertz (GHz) range, presents significant challenges.

These challenges are related to discharge characteristic times, and hence events spectrum, considered in several models, each having a characteristic rise time. For example, slower events such as those characterized by the human-body model (HBM) have a standard rise time of 10 ns [9], equivalent to 100 MHz, which allows passive components like baluns or transformers at the input to effectively filter these events if designed for frequencies near 10 GHz. However, fast discharges following the CDM, defined by their 100 ps rise time, exhibit spectral content extending to frequencies above 10 GHz, and can propagate through the balun, potentially causing severe circuit damage [10], [11]. Consequently, the development of advanced ESD protection design methodologies that ensure both high RF performance and robustness against fast transient events is imperative.

Furthermore, other considerations are critical in circuits such as LNAs, where the additional area and parasitic capacitances introduced by conventional ESD protection devices degrade RF performance at frequencies above the GHz range [12]. Consequently, numerous studies have proposed device-, PAD-, and circuit-level ESD protection solutions focused on minimizing parasitic capacitance while enabling broadband operation. However, these approaches often face limitations such as operation only above 10 GHz, protection targeting solely the HBM model, increased area cost, high parasitic capacitance values, or low CDM current handling capability of the protection strategy [13]–[20].

To mitigate these issues, the impact of additional area and parasitic capacitances requires, at a minimum, the redesign of

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the RF circuit to accommodate these extra parasitic elements, as well as the relocation of conventional components alongside new ESD protection devices. Nevertheless, performance may still be compromised due to the extra losses and noise introduced by these devices [19], [21].

Based on these results, this paper proposes an innovative concept for ESD protection by the integration of diodes within metal , called ”ESD capacitor”. Metal capacitors, which are extensively used in RF circuits for impedance matching and decoupling, offer an unique opportunity to incorporate ESD protection directly into the circuit design due to their simple structure and high Q. This approach not only simplifies the design process by eliminating the need to add separate ESD protection devices after circuit design, but also ensures that protection is inherently integrated from the outset, without any area overhead, while potentially improving the Q and reducing introduced noise compared to standard protections.

In contrast to the work presented in [22], this paper explores the integration of the proposed solution across multiple technology nodes, specifically 28 nm and 18 nm processes. Various design variations are investigated, broadening the applicability of the approach to different use cases. Furthermore, the study includes a detailed analysis of diode miniaturization, as well as a comprehensive experimental procedure encompassing full circuit measurements under ESD events and precise characterization of RF parameters.

The paper is organized as follows: section II introduces the elementary components and discusses the impact of electrostatic discharges across different nodes technologies, focusing on Fully Depleted Silicon On Insulator (FD-SOI) technologies. Section III describes the proposed ESD capacitor, focusing on the integration methodology between the elementary components presented in Section II. This section also covers the ESD behavior of the capacitor, RF parameter extraction, and Q analysis. Section IV presents the application of the component in a LNA, including an evaluation of ESD performance comparing wafer-level and packaged results, as well as its impact on RF performance. Finally, Section V concludes the paper.

II. Technology impact and Elementary components

This section introduces the challenges and impacts associated with different nodes in FD-SOI, as well as the fundamental components involved in the design of the proposed innovative protection scheme.

A. Impact on different FD-SOI nodes

FD-SOI technology, with silicon over buried oxide (BOX) and a fully depleted channel, reduces parasitic capacitances and improves performance and power consumption [23], [24]. In the FD-SOI process, the BOX is a standardized buried oxide insulating layer within the SOI wafer. This layer is fabricated during wafer production and comes pre-integrated. However, FD-SOI requires access to the substrate to manage the back bias of MOS transistors or to fabricate bulk devices. For this purpose, an additional mask is necessary.

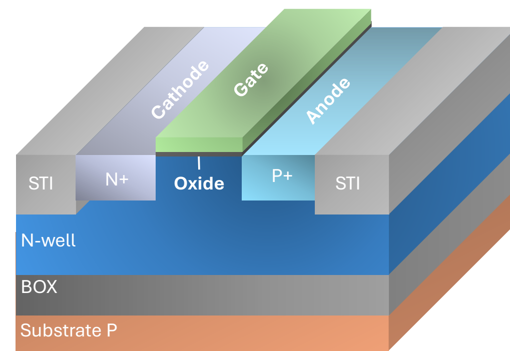

Fig. 1. N-gated diode for ESD protection 3D view.

However, the BOX layer electrically isolates the channel from the bulk substrate, limiting the natural path for ESD current dissipation through the substrate. This necessitates specific ESD protection solutions that account for the reduced capacitance and isolation provided by the BOX.

Among the FD-SOI technology generations, the 28 nm and 18 nm nodes present significant differences that impact ESD protection design. The 18 nm FD-SOI technology, being more advanced and featuring smaller dimensions, offers higher integration density, lower parasitic capacitance, and improved electrical performance compared to the 28 nm node. However, the dimensional scaling also intensifies challenges related to leakage current control and the rapid dissipation of transient charges, requiring an even more refined design of ESD protection devices. Additionally, the BOX layer in more advanced technologies tends to be thinner, which can alter isolation characteristics and parasitic capacitance, directly impacting the effectiveness of commonly used protection solutions (diodes, SCR, ggNMOS) [25], [26]. Thus, the transition from 28 nm to 18 nm FD-SOI technology demands specific adaptations to maintain robustness and efficiency of ESD protection without compromising circuit performance. In conclusion, in the context of ESD protection, FD-SOI technology requires careful design to balance the reduction of parasitic capacitances with the need for efficient energy discharge paths.

Given these technological variations and the challenges associated with the efficient dissipation of transient currents, it becomes essential to explore specialized devices capable of providing robust and fast protection. In this context, gated diodes emerge as an effective solution, integrating a MOS gate structure that significantly enhances the response to ESD events, as detailed in the following subsection.

B. Gated diode ESD protections

Gated diodes are specialized semiconductor devices designed to enhance ESD protection by integrating a MOS gate structure within the diode architecture. The N-gated diode is derived from an NMOS transistor, where the conventional N^+ source is replaced by a P^+ anode [27], as illustrated in Fig. 1.

This diode features a reduced spacing between the MOS gate and the junction regions, which shortens the transit path for minority carriers, significantly improving transient response by reducing voltage overshoot during triggering

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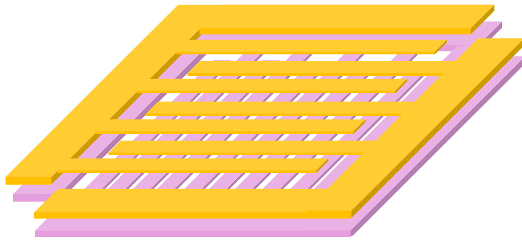

Fig. 2. MOM capacitor 3D view.

events. Furthermore, the enhanced performance is attributed to the MOS gate's ability to confine and control carrier flow, minimizing forward recovery effects. The shorter carrier transit time enables a faster conduction onset, making gated diodes particularly effective against fast and high voltage ESD, such as CDM events [21], [24], [28].

In summary, gated diodes provide a compact and efficient solution for ESD protection in advanced CMOS technologies, combining fast response, reduced voltage stress, and increased robustness, which are critical for safeguarding sensitive integrated circuits. However, these devices exhibit a significantly lower Q compared to components such as capacitors, as discussed in the following section.

C. Metallic Capacitors

Metallic capacitors are key components in RF circuits. One of the main types used is the MOM capacitor, which consists of alternating layers of metal and oxide [29], as illustrated in Fig. 2. These layers are oriented along different axes to optimize capacitance density, compactness, and overall circuit performance. MOM capacitors are widely employed due to their excellent high-frequency characteristics and low manufacturing cost, making them suitable for RF applications [29].

Compared to metal-insulator-metal (MIM) capacitors, MOM capacitors offer advantages such as lower fabrication complexity and cost, since MIM capacitors require additional layers in the manufacturing process. Moreover, MOM capacitors provide high capacitance density, simple layout, and an extremely high Q, facilitating integration in integrated circuit technologies [30].

To enhance the Q of ESD protection, minimize the impact on RF performance, and ensure robust circuit protection, the integration of gated diodes with MOM capacitors is proposed in this paper. This approach is detailed in the following section.

III. Components Integration for ESD Capacitor

Considering the protection capability of gated diodes and the high performance of MOM capacitors in high-frequency applications, an integration of diodes within these capacitors has been implemented. The objective is to preserve the capacitor's Q while providing ESD protection through diodes positioned at the bottom layer, thereby enabling a direct co-design between RF and ESD components [27].

To design and develop the co-design of the ESD capacitor, typical protection mechanisms using gated diodes are

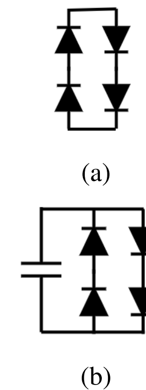

Fig. 3. (a) Secondary protection circuit with four gated diodes and (b) Gated diode network integrated in parallel with MOM capacitor.

considered. A secondary protection circuit based on four gated diodes, as illustrated in Fig. 3(a), is proposed. This circuit is integrated in parallel with the MOM capacitor, as shown in Fig. 3(b). Standard dual diodes provide bidirectional protection and reduce the total capacitance since two diodes are connected in series. Furthermore, the increased trigger voltage makes these devices particularly suitable for ESD protection at LNA input, where signal levels remain close to 0 V. Based on this strategy, efforts are made to miniaturize the ESD components to achieve a compact capacitor with integrated protection, enabling finer capacitance adjustment increments (e.g., 10 fF steps).

A. Gated diode miniaturization

In the optimization of the gated diode capacitance, multiple strategies were implemented to reduce both parasitic capacitances and the intrinsic capacitance of the PN junction, aiming to achieve a significant reduction without compromising device functionality and performance. Initially, considering that the diode capacitance is directly proportional to the PN junction area, the active area was reduced by approximately 90% relative to the original layout, as illustrated in Fig.4. This reduction is critical for lowering the junction capacitance, which depends on the junction area and is inversely proportional to the depletion region width. The decrease in active area results in a proportional reduction in capacitance, which is particularly important for applications requiring low capacitance, such as high-frequency circuits and sensors. However, this reduction must be carefully balanced to ensure that the maximum current handling capability and series resistance remain within acceptable limits, thereby preserving device reliability and performance.

Throughout the optimization process, the gate oxide thickness was maintained constant. Although increasing the oxide thickness could reduce the gate capacitance due to the inverse relationship between capacitance and dielectric thickness, such modification would adversely affect the gate's ability to control the transistor channel, leading to increased threshold voltage and degradation of the device's electrical characteristics. Therefore, preserving the oxide thickness was a strategic decision to maintain the balance between capacitance reduction

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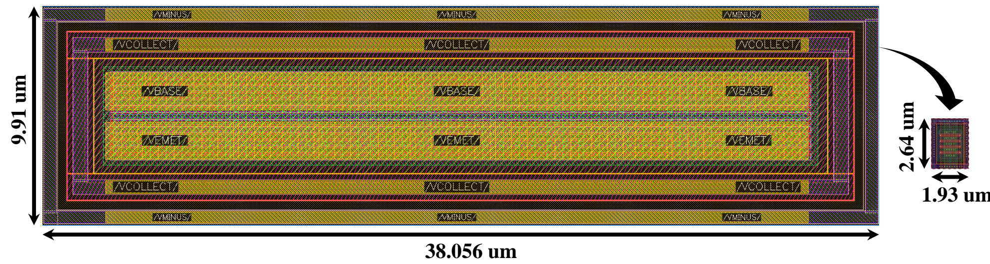

Fig. 4. Reduction of the gated diode active area.

and electrical integrity of the diode.

Finally, the number of metal layers used in the diode contacts was reduced by eliminating four metal levels from the stack. This measure primarily aimed to optimize the parasitic capacitances associated with metal interconnections, since integrating the MOM capacitor in parallel with the diodes allows for a reduction in the number of layers, thereby decreasing the parasitic capacitance.

The combination of these strategies — reduction of metal layers to minimize parasitic capacitances, significant decrease of the PN junction active area to reduce intrinsic capacitance, and preservation of oxide thickness to maintain electrical characteristics — enabled a substantial reduction in the total diode capacitance, approaching the target reduction from approximately 350 fF to values near 5 fF, thereby facilitating the integration of the MOM capacitor as detailed in the following sections.

B. Interconnection between FEOL and BEOL

Once the gated diodes was miniaturized and optimized to be interfaced with the MOM capacitor, the next critical step involved the design of their interconnections with careful consideration of the additional parasitic capacitance and the physical layout constraints. The interconnects must be sufficiently wide to ensure low-resistance current flow during ESD events, while keeping any negative effects on total capacitance and device footprint to a minimum. To achieve this, the four diodes were initially placed as close as possible, sharing the same Shallow Trench Isolation (STI), N-well, and P-substrate regions, as depicted in Fig.5. Subsequently, Metal 1 (M1) and Metal 2 (M2) layers were strategically employed to form the internal connections among the four optimized diodes, as illustrated in Fig.6, thereby creating a routing path to the MOM capacitor while simultaneously connecting the diodes as shown in the 3D view in Fig.6. These metal layers also serve as interface points for the integration with the MOM capacitor structure. The use of M1 and M2 enables a compact routing scheme that reduces parasitic inductance and resistance, thus preserving the high-frequency performance of the co-designed ESD protection network.

Finally, the MOM capacitor was integrated as illustrated in Fig.7. Although the upper metal layers of the MOM capacitor available in the design kit can be utilized, their use is not mandatory. Post-layout extraction showed that the parasitic capacitance contributed by the four gated diodes is approximately 5.3 fF, very near the expected 5 fF. Consequently, an additional MOM capacitor of 4.3 fF, composed of Metal 3 (M3) and Metal 4 (M4) layers was incorporated to achieve a total capacitance of 10 fF, thus constituting the ESD capacitor. This approach enabled the preservation of both the original footprint and capacitance value of a classical 10 fF MOM capacitor, as illustrated in Fig.8.

C. Application strategy of ESD capacitors

This subsection describes the appropriate usage strategy for the implementation of the ESD capacitor within a typical circuit like a LNA. In LNAs functioning at high frequencies, capacitor values commonly reach up to several tens to hundred femtofarads, with equivalent impedance generally near 50 Ω. However, replacing passive components with active ones can introduce additional noise due to the low Q of these active devices. Therefore, it is fundamental to verify that the proposed strategy minimizes introduced noise.

The Q for a device of impedance Z is defined as :

$$Q = \frac{\mathrm{Im}(Z)}{\mathrm{Re}(Z)}, \tag{1}$$

where $\mathrm{Im}(Z)$ and $\mathrm{Re}(Z)$ represent the imaginary and real parts of the impedance, respectively. In the ideal case of a capacitor, the equivalent series resistance (ESR) tends to zero, resulting in a Q approaching infinity. It is therefore to minimize the internal resistance of the device as much as possible.

Based on this, instead of using large ESD capacitors, a mosaic arrangement composed of 10 fF capacitors connected in parallel was implemented. This configuration allows the total capacitance to be increased to the desired value while simultaneously reducing the equivalent internal resistance, since the resistances of the capacitors in parallel combine to decrease the total effective resistance.

D. Configurations and technology nodes variations

Various design variations were explored across different semiconductor technology nodes to evaluate the performance and effectiveness of ESD protections integrated into RF LNA circuits under diverse operating conditions. Initial studies were

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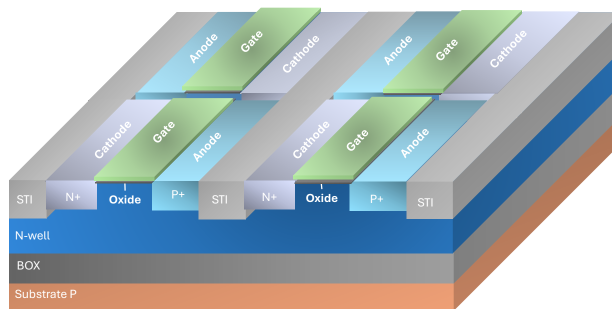

Fig. 5. 3D view of the four miniaturized gated diodes sharing STI, N-well, and P-substrate.

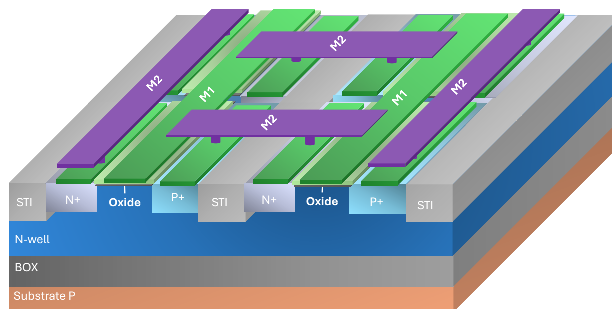

Fig. 6. 3D view of the gated diodes with Metal 1 and Metal 2 interconnections.

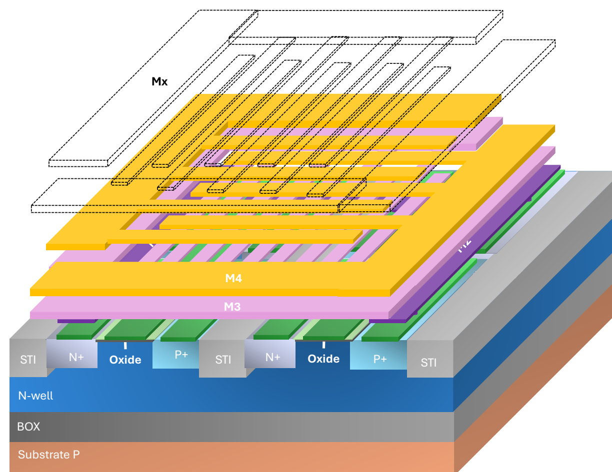

Fig. 7. 3D view of the MOM capacitor with the gated diode integrated to form the complete ESD protection capacitor.

conducted using the C28FD-SOI technology from STMicroelectronics, chosen for its superior performance and energy efficiency.

In the FDSOI technology, various ESD capacitor variations are implemented for study, covering different capacitance values and different connection configurations between the structures. Initially, work is performed at the 28 nm node, where the initial version of the 10 fF capacitor is used. From this initial approach, ESD capacitors with values of 10 fF, 350 fF, and 1 pF are integrated. These values are strategically selected: 10 fF as the smallest available value, 350 fF as it is used as the ESD capacitor in the use case of the following section, and 1 pF for Q analysis.

Within the same technology, a variation of the ESD capacitor is explored, where instead of connecting multiple 10 fF capacitors in parallel, larger-area unitary capacitors with integrated large-size diodes are adopted. This configuration aims to increase the energy dissipation capability during ESD events. For this variation, capacitors with values of 350 fF and 1 pF are integrated, allowing comparison with the original versions and evaluation of the trade-offs associated with the new concept.

Subsequently, the ESD protection is integrated in the 18 nm technology node, presenting two main variations. The first corresponds to the initial version, with 10 fF capacitors connected in parallel, where values of 36 fF and 1 pF are integrated. The 36 fF capacitor is chosen for ESD testing due to the trend of integrating more compact circuits at this node, while the 1 pF

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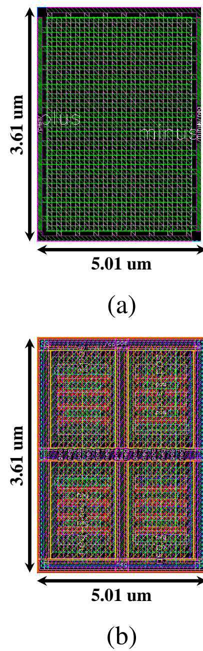

Fig. 8. (a) 10 fF MOM capacitor layout and (b) 10 fF ESD capacitor layout.

TABLE I
SUMMARY OF ESD PROTECTION DESIGN VARIATIONS

ID	Technology Node	Capacitance Values	Configuration
1	28 nm	10 fF, 350 fF, 1 pF	Parallel connection
2	28 nm	350 fF, 1 pF	Single connection
3	18 nm	36 fF, 1 pF	Parallel connection
4	18 nm	36 fF, 1 pF	Series connection

capacitor is used for Q evaluation and comparison with the previous version.

The second variant consists of increasing the number of diodes connected in series to improve voltage triggering tolerance. This configuration is particularly relevant for power amplifier (PA) applications, where robustness against voltage spikes is critical. In this variant, ESD capacitors of 36 fF and 1 pF are integrated to enable direct comparison with the initial version.

Table I summarizes all protection variations, integrated capacitance values, design descriptions, and device nomenclature.

E. Characterization

To validate the device studies, characterization of the ESD protection devices was performed through electrical measurements and specific tests. This includes the methods used for capacitance extraction, Q analysis, and evaluation of device behavior under ESD tests (TLP and VF-TLP). These results are essential to understand the device performance in high-frequency applications and their effectiveness in protecting against ESD events.

1) RF measurement for capacitance extraction: Parasitic capacitance extraction is a fundamental process in the design and analysis of integrated circuits, especially for RF applications. Parasitic capacitances arise due to the physical geometry of

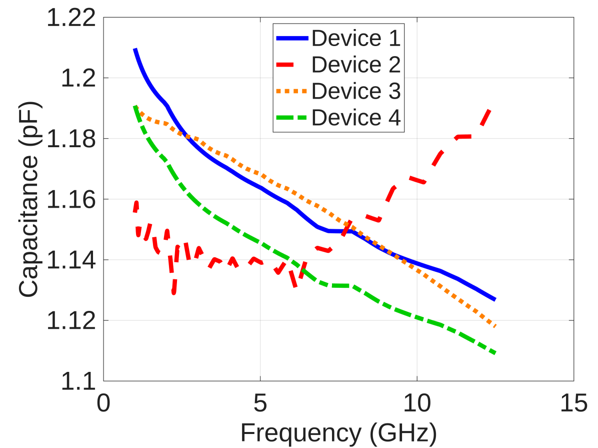

Fig. 9. Measured capacitance versus frequency for the four ESD protection devices.

devices, interconnections, metal layers, dielectrics, and the proximity of conductors in the chip layout. These parasitics can significantly affect circuit performance.

The parasitic capacitance extraction for devices such as ESD capacitors is performed by measuring S-parameters using a vector network analyzer (VNA) over a frequency range of 0.5 to 15 GHz. These parameters are then converted to admittance, where the imaginary part corresponds to the capacitances. To isolate the intrinsic device capacitances, a de-embedding technique is applied to remove the effects of pads and interconnections. Subsequently, an equivalent circuit model including capacitive elements is numerically fitted to the measured data, enabling precise extraction of the parasitic capacitances. It is important to consider that these capacitances vary with frequency, bias voltage, and device geometry, all of which directly impact the component's performance in high-frequency applications.

For the devices under study, the extracted parasitic capacitance, for the ESD capacitors of 1 pF, given in Fig. 9. Devices 1 and 3 exhibit slightly higher capacitance values with a gently decreasing trend as frequency increases, indicating a stable and predictable response of high quality capacitors suitable for RF applications. Device four shows slightly lower capacitance values with a similar decreasing trend, which may indicate a smaller effective area or structural differences in the capacitor, yet remains within a stable range. Conversely, Device 2 presents a more irregular behavior, with variations and even an increase in capacitance above 10 GHz, suggesting possible parasitic effects or resonances associated with the configuration involving larger integrated diodes.

2) Quality factor: An ideal capacitor, characterized by a finite series resistance, can be modeled as a series RC circuit exhibiting a single-pole frequency response [31]. The Q of the capacitor is inversely proportional to this series resistance; therefore, a higher Q indicates lower resistive losses. ESD protection circuits, in their "off" state, are designed to block DC current flow, inherently behaving as capacitive elements with series resistance similar to that of an ideal capacitor [31].

To achieve a high overall Q in an ESD protection device, it is essential to minimize the series resistance associated

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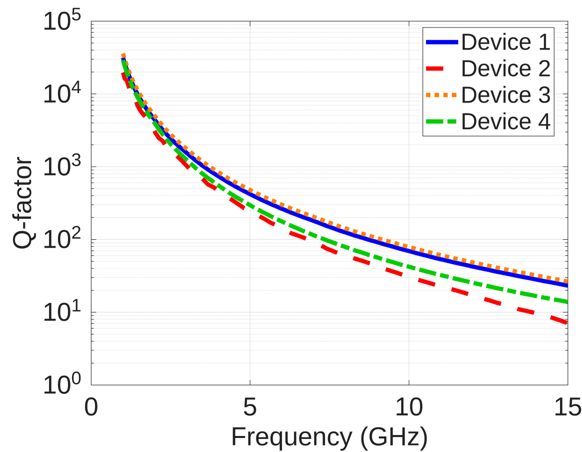

Fig. 10. Q of the ESD devices as a function of frequency.

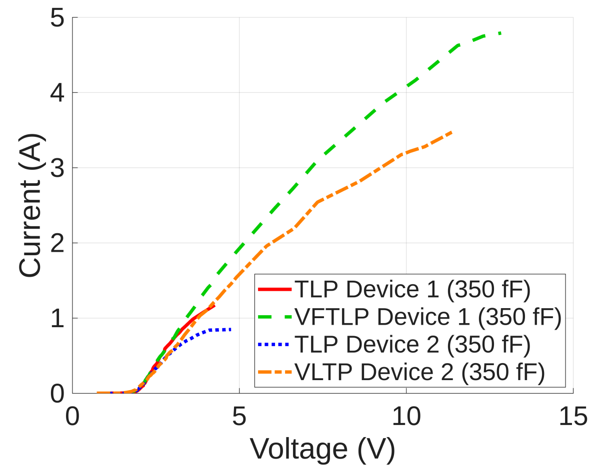

Fig. 11. Current-voltage characteristics of devices 1 and 2 with 350 fF capacitance under TLP and VF-TLP stress tests.

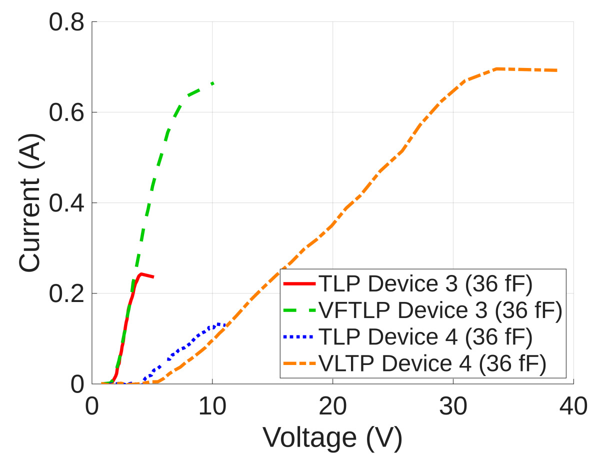

Fig. 12. Current-voltage characteristics of devices 3 and 4 with 36 fF capacitance under TLP and VF-TLP stress tests.

with the dominant capacitive element, which corresponds to the largest capacitor in the single-pole model. The design challenge lies in adjusting the network's poles and zeros so that, within the frequency range of interest, the protection circuit approximates a single-pole capacitive response with a maximized Q.

Fig. 10 shows the measured Q as a function of frequency for the four studied ESD protection devices. The results demonstrate that all devices maintain a Q greater than 10 up to 15 GHz (except for Device 2, 13 GHz). Notably, around 10 GHz, Devices 1 and 3 achieve Q values close to 90, approaching the performance of high-quality MOM capacitors, which typically exhibit Q near 100. Devices 2 and 4, which incorporate large integrated diodes and series diode configurations, respectively, exhibit slightly lower but still robust Q factors, indicating effective capacitive behavior with minimal resistive losses.

These results confirm that the proposed ESD protection designs provide high Q capacitive characteristics essential for minimizing insertion loss and preserving RF performance in sensitive circuits such as LNAs. Among the configurations analyzed, the parallel capacitor designs (Devices 1 and 3) demonstrate superior Q performance, making them the preferred choice for high-frequency ESD protection applications.

3) TLP and VF-TLP characterization: The TLP test is a widely used technique to characterize the behavior of components and circuits under stress conditions. Typical pulses have a duration of approximately 100 ns, with current levels reaching several amperes. After each TLP pulse, a low-current DC measurement is usually performed to determine whether the device under test (DUT) has been damaged by the preceding pulse. Changes in the DC measurement results often indicate device damage [32]. This testing method enables components to be subjected to electrical stress similar to that caused by HBM discharges, with the energy released by a TLP pulse being comparable to that of an HBM event.

To measure high-current and fast rise time conditions to evaluate the ESD devices performances for fast CDM event, very-fast TLP (VF-TLP) testing uses a pulsed voltage source combined with a high-impedance connection to the DUT, generating pulses approximately one nanosecond in duration with rise times on the order of a few hundred picoseconds [27].

The VF-TLP measurement method of the TDRS-T (High-Z Time Domain Reflection Separate and Transmission) type employs a setup similar to conventional TLP but uses a "Pick Off Tee" to measure current instead of a probe.

The four ESD devices with different technology versions and architectures described in Table I, were evaluated through TLP and VFTLP tests.

Devices 1 and 2 have a nominal capacitance of 350 fF, both fabricated using 28 nm.

In Fig. 11, which presents the results for the 350 fF devices, it can be observed that Device 1 supports higher currents in both tests, reaching nearly 5 A in the VF-TLP, as compared to around 3.5 A for Device 2. This difference indicates that the configuration with ESD capacitors connected in parallel, as in Device 1, offers better current handling capability. Conversely, Device 2, which incorporates only a single cell, exhibits a limitation in the maximum current supported, although this architecture may provide advantages in terms of overshoot reduction, as observed in the TLP test, show in Fig.. 11. This behavior is consistent across both TLP and VF-TLP tests.

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Devices 3 and 4, both with a capacitance of 36 fF and fabricated using 18 nm technology, have different architectures but support similar currents in the VF-TLP test, reaching approximately 0.7 A. The strategy of increasing series diodes in Device 4 offers additional protection against voltage triggering, making it a suitable solution for high-power RF applications, such as PAs. This pattern is also observed in the TLP test results.

When comparing devices with the same capacitance, architectural differences directly impact the supported current capacity and behavior under ESD transients. However, even with similar architectures, devices fabricated using 28 nm technology demonstrate slightly superior robustness against ESD events, supporting higher currents than devices fabricated with the 18 nm technology. This increased robustness can be attributed to metal backend option.

IV. Use case: LNA application

To deepen the analysis of the proposed devices, they were integrated into an LNA. Device 1 was selected for integration due to its high Q and proven robustness against ESD events.

The circuit depicted in Fig. 13(a) represents the use case: a cascode LNA designed to operate in the 6 to 12 GHz frequency range, implemented in STMicroelectronics' 28 nm C28FD-SOI technology. A transformer was inserted at the circuit input to ensure impedance matching and primarily to act as a filter for protection against ESD events modeled by the HBM, which typically occur at low frequencies around 100 MHz. The main objective of this study was to evaluate the robustness of the proposed solution under various electrostatic stress conditions. To this end, VF-TLP characterization and qualification tests using CC-TLP discharges were performed at the circuit's RF input pin.

Two distinct protection configurations were analyzed to validate the effectiveness of the proposed solution: (1) a configuration without secondary protection, containing only the transformer and clamps, as illustrated in Fig. 13(a); and (2) a configuration with optimized ESD capacitors replacing only C1 and C3, achieving a balance between ESD robustness and RF performance within the operating band without modifying the basic structure of the LNA, as shown in Fig. 13(b), however, using ESD capacitor values different from those in the version of Fig. 13(a) with the aim of optimizing ESD performance.

The cascode topology was chosen for the LNA due to its simplicity and widespread use in RF circuits, as well as its ability to provide high performance. Additionally, this topology is more vulnerable to ESD discharges because it has a direct path to the transistor gate, making the study and implementation of ESD protections especially relevant and challenging in this context.

Another important aspect is that ESD capacitors, although highly efficient for protection, can degrade the LNA's performance when sized to provide maximum protection. This highlights the trade-off between protection effectiveness, performance degradation, and increased chip area. Thus, the ESD capacitor is extremely efficient, but the value that ensures maximum protection does not always coincide with the one that best meets RF performance requirements. The choices made to increase the value of the ESD capacitors, replacing the MOM capacitor, aim to balance these factors, ensuring adequate protection without compromising RF performance and project area.

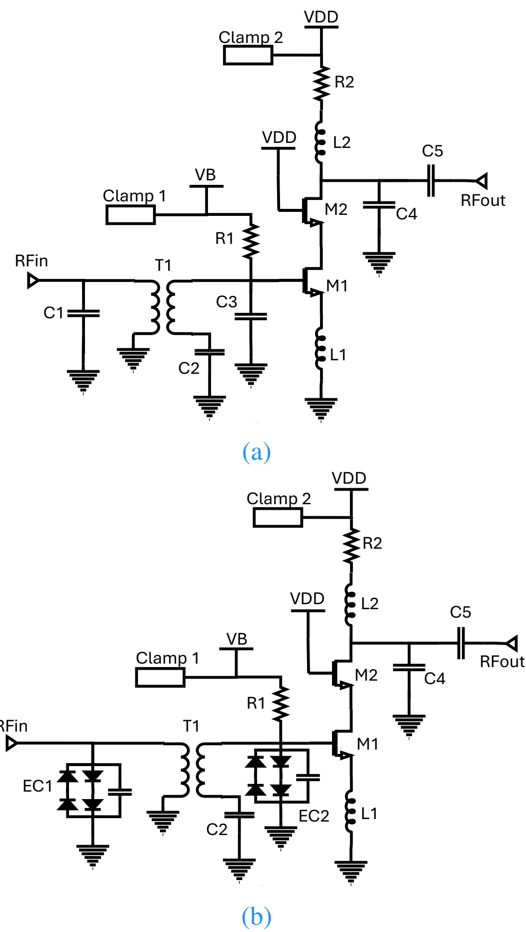

Fig. 13. Schematics circuits of the LNAs : (a) Without secondary protection (Circuit 1) and (b) ESD capacitors (Circuit 2).

Following the design and layout of both configurations, the RF performance was rigorously evaluated to quantify the impact of each approach. The detailed results include critical parameters such as input matching, where the protections are implemented, gain, and noise figure (NF).

It is important to note that in CMOS LNAs, ESD protection is typically positioned near the input region of the circuit, specifically close to the transistor gate, which is the most vulnerable part of the system. Consequently, the input matching parameters are significantly more affected compared to those of the output. Additionally, the amplifier gain and noise figure are also impacted, as the active devices involved in the protection can introduce additional losses, noise, and alter the overall circuit performance.

A. Oxide failure condition

In the context of LNA applications, it is important to understand the failure mechanisms of transistors fabricated

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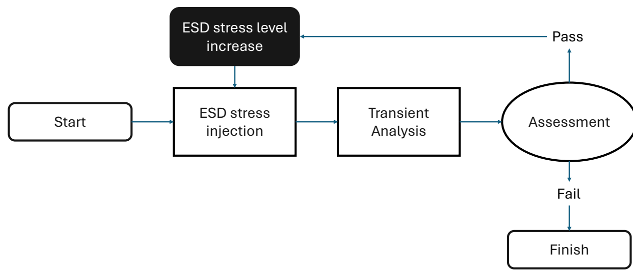

Fig. 14. Schematic of the LNA use case and simulation setup.

with C28FD-SOI and bulk 28 nm technologies. In these technologies, the NMOS transistors employed in the LNA exhibit a critical gate-to-source voltage (V_{GS}) limit of 4.5 V. Exceeding this threshold results in gate oxide breakdown, causing transistor failure. For simulation purposes, V_{GS} was continuously monitored under stress conditions.

Fig. 14 depicts the block diagram of the simulation setup. The procedure begins with the injection of ESD into the system. This stress is subjected to transient analysis to evaluate the system response. Following the analysis, a pass/fail assessment is performed. If the system fails, the process terminates and the maximum ESD current is recorded; otherwise, the ESD stress level is incremented and the cycle repeats.

The input current to the circuit is monitored for each applied voltage. During stress application, the V_{GS} of transistor M1 is measured. When V_{GS} reaches or exceeds 4.5 V, the circuit is considered to have failed due to gate oxide breakdown. This threshold indicates that the LNA cannot withstand the applied stress, resulting in degradation of key RF parameters. This simulation methodology ensures an accurate assessment of the LNA's robustness and helps identify critical failure points, providing valuable insights for designing more resilient circuits.

The measurement analysis methodology differs from the simulation approach. Although the circuit was stressed at the input similarly to the simulation, direct measurement of V_{GS} is not feasible due to lack of access to the transistor's gate and source terminals due to the transformer DC filtering. Consequently, an alternative approach was developed with the analyzes of the VDD current (I_{VDD}). The analysis procedure is as follows: a DC measurement is performed prior to stress application to establish a baseline VDD current. Subsequently, stress is applied, and the VDD current is monitored immediately afterward to detect any changes, as illustrated in Fig. 15.

The process continued until a significant alteration in I_{VDD} was observed. Since the VDD current is strongly correlated with the transistor's operating conditions, any variation in I_{VDD} effectively indicates changes within the transistor or circuit behavior. This methodology enables detection of transistor stress effects through indirect measurement of the VDD current, providing a reliable means to assess the impact of stress on the circuit.

A similar analysis can also be performed using the bias current (I_{bias}), as it is closely related to the transistor's gate voltage and operating point. Monitoring either current provides

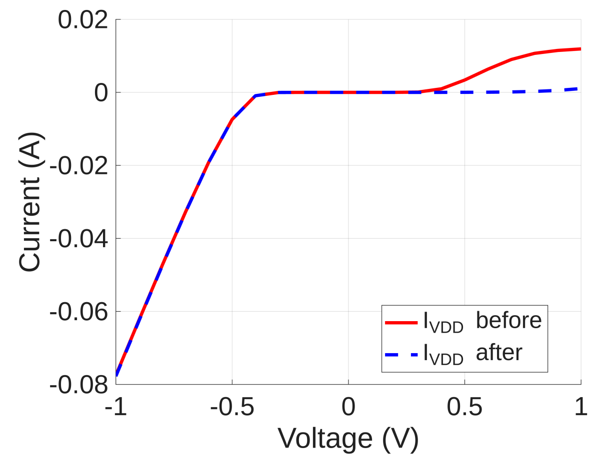

Fig. 15. Variation of VDD current (I_{VDD}) before and after stress application.

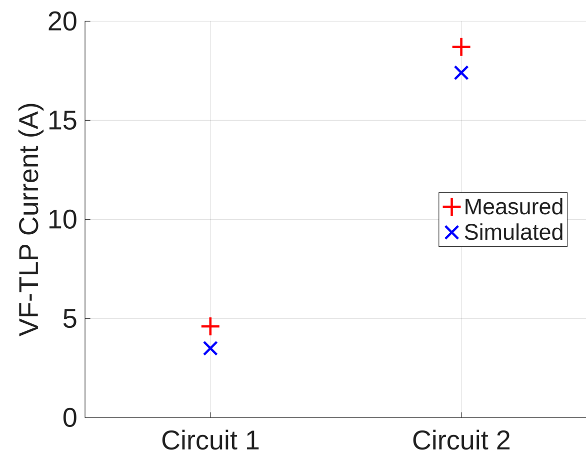

Fig. 16. Breakdown current comparison for the VF-TLP test across different circuit configurations.

complementary insight into the stress induced changes in the device.

B. VF-TLP

For the VF-TLP test, the two circuit versions were simulated and measured until failure occurred. The results, presented in Fig. 16, show that the unprotected circuit (Circuit 1) fails at a breakdown current below 4 A, indicating transistor burnout. In contrast, Circuit 2, which incorporates the ESD capacitor, demonstrates high resilience to high-level discharges, failing only at currents close to 17 A, thus evidencing the effectiveness of the proposed protection concept. An excellent agreement between simulation and measurement results is observed, validating the predictive capability of the ESD robustness for each variant.

C. CC-TLP

While VF-TLP applies two-pin stress with defined input and output contacts, CC-TLP connects only the hot pulse terminal directly to the DUT. The CC-TLP test tip connects to a rigid transmission line coupled to a ground plane, forming a parasitic capacitance between the ground plane and the tested

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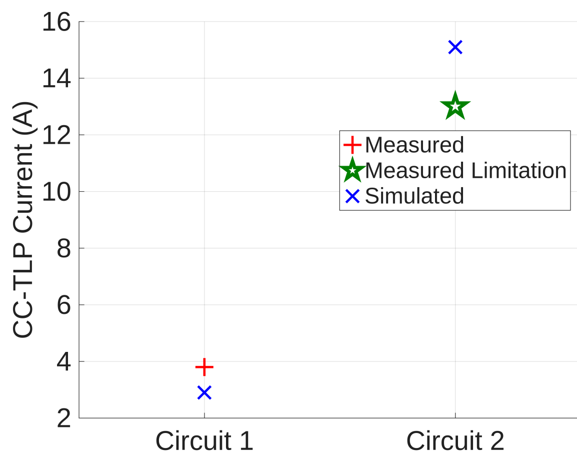

Fig. 17. Breakdown current comparison for the CC-TLP test across different circuit configurations.

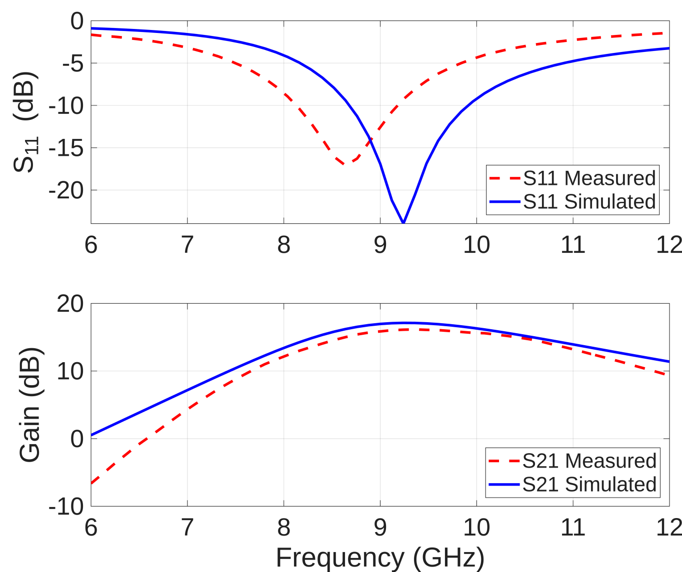

Fig. 18. Simulated and measured S-parameters for the standard LNA configuration.

component. Measurements can be done on silicon wafers or packaged devices. This capacitance corresponds to the background capacitance of a packaged device, which charges and discharges during CDM stress events, indicating a closer correlation between CC-TLP and CDM stress.

The results are presented in Fig. 17 for the CC-TLP, performed on wafer. The unprotected circuit fails at approximately 4.8 A during measurements and around 3.7 A in simulations. This discrepancy can be attributed to measurement inaccuracies due to the large voltage difference between two consecutive measurement steps.

Conversely, the ESD capacitor demonstrates remarkable robustness under high discharge conditions, with a simulated failure threshold of approximately 15.1 A. It was not possible to reach this failure current during measurements due to the maximum current limit of the instrument. However, the measurement results show that the ESD capacitor protection is capable of absorbing currents exceeding 13 A, which was the maximum current that could be applied in the CC-TLP test due to the limitation of the measuring instrument.

These results further emphasize the robustness of the proposed ESD protection concept.

D. RF impact with different configurations

The study and analysis of the impact on RF performance caused by different ESD protection configurations is essential. It was carried out through simulations and measurements of S-parameters and noise figure (NF), evaluating how the inclusion and optimization of ESD capacitors the overall circuit behavior.

1) S-Parameters: to perform the RF measurements of the LNA, specific instruments and procedures were employed depending on the circuit type. A vector network analyzer Agilent 8510C, coupled with an Agilent 8515A test set and an HP 83631B synthesized signal generator, was used, supplemented by a second HP 8514A test set. Calibration was carried out using dedicated kits applying the full two-port (SOLT) method to correct systematic errors and ensure measurement accuracy. These measurements were conducted on a test station equipped with model 1034X microwave probes, utilizing various types of high-precision coaxial probes (GSGSG, GSG, or GS) to ensure optimal electrical contact and minimize parasitic losses.

In the standard LNA configuration, as shown in Fig. 18 (a), the simulation results indicate excellent input impedance matching near 9 GHz, evidenced by a minimum S_{11} value around -24 dB. The measured data corroborate this trend, showing a similar minimum, although with a slightly reduced reflection of about -17 dB. This minor discrepancy is attributed to parasitic effects that are not fully captured by the simulation models. The maximum simulated gain reaches approximately 16 dB at 9 GHz, while the measured gain peak is slightly lower, close to 14 dB, exhibiting a relatively flat response throughout the operating band. This strong agreement validates the standard model for applications where RF performance is paramount.

With the introduction of optimized ESD capacitors, designed to enhance robustness against electrostatic discharge events while maintaining good LNA performance, Fig. 19 (b) illustrates a slight change in the S_{11} minimum to around 8 GHz. The simulation shows a deeper minimum near -21 dB, indicating an adjusted impedance matching point. However, the measured reflection is somewhat less pronounced at approximately -16 dB, revealing additional losses and parasitic effects not fully taken into account in the simulation. The maximum simulated gain in this configuration is about 15 dB, closely matched by the measured peak near 14 dB, although the measured gain exhibits a steeper roll-off outside the peak frequency. These results confirm that increasing the value of the ESD capacitor, which replaces the original metal capacitors, slightly shifts the RF behavior response relative to the standard circuit model, as expected from the simulation. Furthermore, the frequency shift can be corrected by improving the ESD capacitor model.

The comparison between simulation and measurement demonstrates good performance with the proposed protection. Furthermore, the standard model maintains near-ideal

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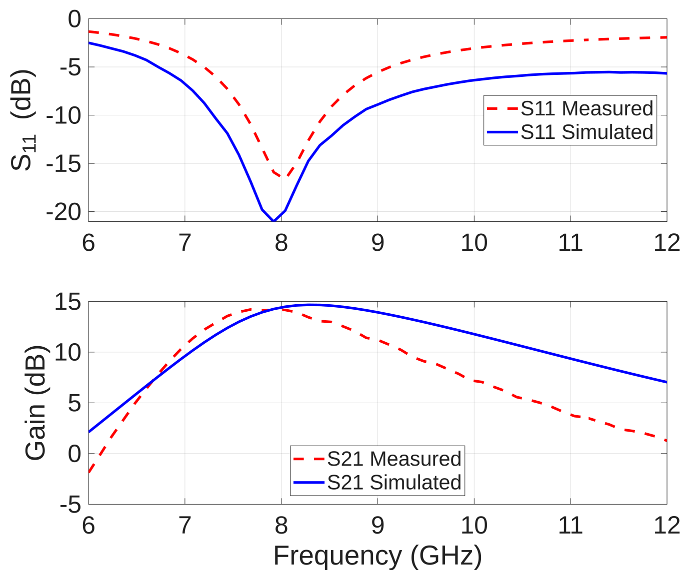

Fig. 19. Simulated and measured S-parameters for the LNA configuration with optimized ESD capacitors.

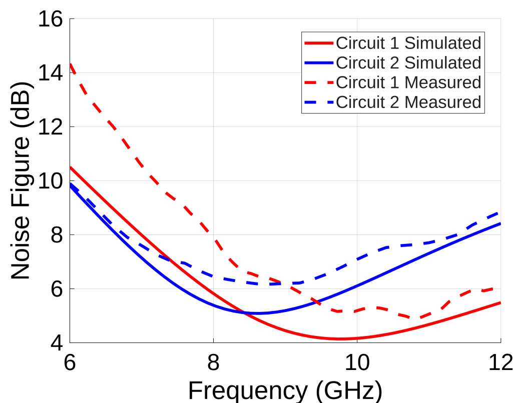

Fig. 20. Simulated and measured NF for the LNA configurations.

performance, the ESD-protected configuration exhibits only minor degradations, mainly due to the complexity of additional passive elements and their interactions within the physical layout.

2) Noise figure: Regarding the NF, Figure 20 shows that both circuits exhibit a decrease in NF as the frequency increases from 6 GHz up to approximately 9 GHz, where the NF reaches its minimum values, followed by an increase up to 12 GHz. Circuit 1 (without ESD capacitors) demonstrates a simulated minimum NF of approximately 4 dB, while the measured value is around 5 dB, indicating a 1 dB increase due to practical factors. Similar to the S-parameters, the NF of circuit 2 (with ESD capacitors) shows a frequency shift compared to circuit 1, with a simulated NF of 5 dB and a measured NF of 6 dB. The behavior of both circuits is similar when comparing their measured and simulated values, which is a positive indication of the consistency and reliability of the results.

V. Conclusion

This work presents a novel ESD protection approach that integrates gated diodes within MOM capacitors, achieving a compact device with a high Q and enhanced robustness, suitable for RF circuit protection in advanced CMOS technologies. The proposed ESD capacitor maintains excellent RF performance while providing effective protection against fast transient events, as validated by extensive TLP, VF-TLP, and CC-TLP characterizations.

Integration into a 28 nm FD-SOI technology LNA demonstrated minimal impact on key RF parameters. In the standard LNA configuration, the S_{11} parameter exhibits a minimum near -24 dB (simulated) and -17 dB (measured) at 9 GHz, with a gain of approximately 16 dB (simulated) and 14 dB (measured). With the optimized ESD capacitors, the S_{11} minimum shifts to 8 GHz, with values around -21 dB (simulated) and -16 dB (measured), while the gain remains close to 15 dB (simulated) and 14 dB (measured).

Additionally, a significant improvement in ESD robustness was observed, with failure currents exceeding 15.1 A in simulation and above 13 A in measurements—approximately three times greater robustness in the optimized circuit compared to the standard one. Moreover, the ESD capacitor exhibits an impact on the LNA circuit that is consistent with the expected effect on gain within the 6 to 12 GHz frequency range, with measured values closely matching the simulated behavior. This is attributed to the high Q of the ESD capacitor and the parallel configuration of multiple capacitors, which minimize resistive losses and parasitic capacitances, thereby preserving the performance of the circuit even with the integrated protection.

These results confirm the viability of the proposed protection scheme for next-generation high-frequency applications, offering a promising solution to combine ESD reliability with stringent RF performance requirements without compromising area or performance. Furthermore, the solution enables not only the integration of gated diodes but also other components such as STI diodes and ggNMOS devices, along with various internal connection configurations— including the use of series diodes with a central connection—allowing adaptation to a wide range of applications.

VI. Acknowledgment

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