A 79 GHz 4-Way Power Amplifier with 23 % PAE and 30dB Gain in 28nm CMOS

Oumayma Belkhadra, Gilles Montoriol, Manuel J. Barragan, Salvador Mir, Florent Cilici, Emmanuel Pistono, Sylvain Bourdel

A 79 GHz 4-Way Power Amplifier with 23 % PAE and 30 dB Gain in 28 nm CMOS

Oumayma Belkhadra[1,2], Gilles Montoriol[1], Manuel J. Barragan[2], Salvador Mir[2], Florent Cilici[1], Emmanuel Pistono[2], and Sylvain Bourdel[2]
[1]*NXP SEMICONDUCTORS, Toulouse, France*
[2]*Univ. Grenoble Alpes, CNRS, Grenoble-INP, TIMA*

***Abstract*—This paper presents a 79 GHz 4-way Power Amplifier in 28 nm CMOS technology designed for maximum efficiency. Each unit amplifier has three stages: a neutralized cascode pre-driver, followed by neutralized common source driver and output stages. The PA achieves a measured linear gain of 30 dB, a saturated output power of 17 dBm, and a 1-dB compression point of 10 dBm. This design offers a suitable trade-off between power consumption, size and output power. To the author's knowledge, the obtained PAE of 23 % is the highest among sub-65 nm CMOS technologies for automotive radar applications published in the literature.**

***Index Terms*—power amplifier, combiner, CMOS, radar, integrated circuits**

I. Introduction

The high level of integration of CMOS technologies has allowed them to be used extensively in millimeter-wave applications. However, if we consider the design of Power Amplifiers (PAs), the low values of the transistor breakdown voltage and Fmax in these technologies limit the achievable PA gain and output power. To tackle this problem, three main techniques are employed. First, larger transistors increase PA output current, but complicate impedance matching and increase insertion loss and parasitic capacitance, impacting area. Second, the stacked-FET approach, described by [1], raises output voltage above breakdown voltage, but hampers gain and PAE, due to gate to ground capacitors. Third, the power combination technique based on integrated transformers [2] is widely used for compactness and minimal insertion loss, offering the best solution to reduce impedance transformation ratio and to increase output load impedance [3]. Increasing the number of combined PA ways boosts output power and load impedance at the expense of increasing phase imbalance issues. To minimize these issues in the n-way PA, the number of combined ways must be limited.

Recent studies highlight the considerable diversity in amplifier designs, particularly in the number of stages in the Unit Amplifier (UA), and the types of amplifier structures used to build each stage. Commonly used structures include Neutralized Cascode and Common Source (respectively, NCA and NCS) topologies [4]–[7]. NCA provides high power gain, while NCS offers optimum efficiency and good reverse isolation. The Neutralized Bootstrapped Cascode Amplifier (NBCA) topology enhances power gain and output power while maintaining stability [6]. Different arrangements of PA stages have been explored in the literature as it can be seen in Table II. In [7], two NCS followed by one NCA allows to reach 29.7 dB gain and 22.1 % PAE, while in [4], 2 NBCA stages demonstrate the highest PAE of 22.3 %. It appears that choosing the best architectures and the best number of stages regarding specification is a hard task leading to various trade-offs.

In this work, we present a novel Unit Amplifier (UA) configuration never reported so-far, composed of a NCA followed by two NCS stages in order to implement a high efficiency 4-way PA in a 28 nm CMOS technology. The NCS topology is adopted for the driver and the output stages for its good efficiency. The pre-driver stage is realized by a NCA architecture to alleviate the high PA input transformation ratio and the low input power requirements. The proposed PA achieves good measured performances such as PAE of 23 %, G_p of 22 dB and P_{sat} of 17 dBm at 79 GHz. In the rest of this paper, Section II describes the PA design, including the output power combiner and input power splitter. In section III, experimental results are compared to the state-of-the-art of 4-way PAs implemented in CMOS technologies below 65 nm targeted at applications above 60 GHz. Finally, Section IV summarizes our contributions and discusses future work.

II. Power Amplifier Design

The schematic of the proposed PA is shown in Fig. 1. It has been designed and fabricated in a 28 nm CMOS technology. Its architecture consists in a four-identical-way power combining amplifier with 50 Ω input matching. It adopts a pseudo-differential architecture to reduce even harmonic distortion and improve common-mode rejection.

A. Design of a PA unit

Each way is implemented as a 3-stage UA. The UA study proceeds from the last (output) to the first (pre-driver) stage. The target output power of the last stage is approximately 9 dBm. The preceding stage power is calculated with a 3-dB margin to prevent premature compression as

$$P_{driver} = P_{out} - G_{out} + L + 3\,\text{dB} \tag{1}$$

where G_{out} is the output stage power gain and L is the interstage matching insertion loss. Since the output and driver stages determine the pre-driver requirements, they are studied first. To take advantage of the various common topologies (i.e., NCS, NCA or NBCA) while mitigating their drawbacks, different combinations of these structures have been studied, leading to different trade-offs in terms of gain, impedance and

linearity. In this work, we have compared different topology combinations using the aforementioned structures to find the one that maximizes the PAE of a two-stage UA as presented in Table I. Our analysis (reported in Table I) is based on load pull simulations using the PDK transistor models and accurate transformer models. An NCS topology in both driver and output stages yields the highest PAE.

TABLE I
SIMULATION RESULTS OF DIFFERENT ARCHITECTURE COMBINATIONS FOR A 2-STAGE UNIT AMPLIFIER

		G1	G2	DE1	DE2	Loss	PAE_{global}	$Gain_{global}$
Driver	Output	dB	dB	%	%	dB	%	dB
NCS	NCS	7.8	7.8	39.3	39.3	2	29.76	13.6
NCA	NCA	8.8	8.8	25.7	25.7	2	20.72	15.7
NCA	NCS	8.8	7.8	25.7	39.3	2	27.06	14.6
NBCA	NBCA	10	10	21.51	21.51	2	18.27	18
NBCA	NCS	10	7.8	21.51	39.3	2	25.85	15.8

In NCS, a high neutralization capacitor value leads to PA oscillation and drastically decreases the source impedance [8]. This results in an increase of the inter-stage matching transformation ratio and the degradation of its insertion loss. Thus, the capacitor value represents a trade-off between stability and source impedance on one hand, and power gain on the other hand. In addition, neutralization provides unilateralism which has to be considered in the capacitor sizing.The UA output stage measures 76.8 µm, while the driver stage is 57.6 µm.

A low source impedance is the main drawback of a NCS topology. The higher the capacitor value, the lower the impedance. As a result, in order to minimize the insertion loss of the power splitter at the input and reduce its transformation ratio, a pre-driver stage implemented in a NCA configuration is added. The NCA topology has a source impedance two times higher than the common source topology, and its efficiency has a negligible impact on the global UA efficiency given by

$$PAE_{UA} = \frac{G_3 L_2 L_1 G_2 - 1/G_1}{1/DE_1 + (L_1 G_2)/DE_2 + G_3 L_1 L_2 G_2/DE_3} \quad (2)$$

where the index i is 1 for the NCA pre-driver, 2 for the NCS driver and 3 for the NCS output. G_i and DE_i refer, respectively, to the power gain and drain efficiency, while L_i represents the loss of the i^{th} inter-stage matching.

To maximize each stage power gain, the width of the transistor finger is fixed for the maximum transition frequency defined by Mason invariant

$$U = \frac{|Y_{21} - Y_{12}|^2}{4 * (Re(Y_{11}) * Re(Y_{22}) - Re(Y_{12}) * Re(Y_{21}))} \quad (3)$$

where $U(F_{max}) = 1$. To set a proper V_{gs} value of each UA stage and alleviate the trade-off between PAE and output power, load-pull simulations are performed. For the inter-stage matching, integrated transformers are adopted to minimize the overall size of the system. In addition, their midpoint serves a double purpose of representing a virtual ground and enabling the DC bias of active devices.

B. Design of power combiner and splitter

The input signal is split to drive two transformer-based power dividers and split again to form the 4-ways. To prevent current leakage to the substrate, the TL adopts a slow wave configuration. It minimizes the losses [9] and shields the RF signal from the lossy substrate. The shielding lines are implemented in metal M3 to ease the routing of supply and ground signals underneath. The implemented TL displays 0.25 dB of insertion loss at 79 GHz.

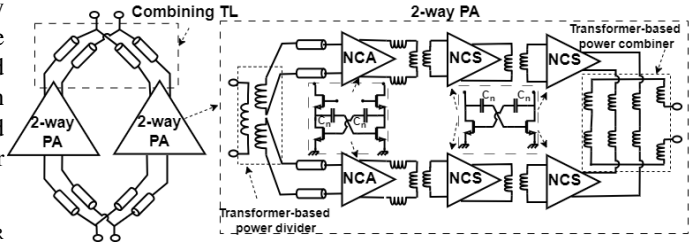

Fig. 1. Schematic of the proposed 4-way PA

The output power combiner is based on the same configuration proposed in [6], implemented in 40 nm CMOS technology. It incorporates two transformer-based power combiners and a combining TL. Our transformer based power combiner is configured with two differential inputs represented by two half primary windings. They are implemented in the two thick stacked metals M7 and M8. This technique increases the coupling coefficient as well as the quality factor, and helps reducing the insertion loss. As seen in Fig. 2b, the two half primary windings are connected by a tap-bar through the two midpoints of the power combiner. This allows an equipotential biasing of the two combined PA output stages. The secondary winding is implemented in the thickest layer AP, featuring a very low resistivity. Additionally, the interconnection between the UA output and the combiner is minimized to reduce insertion losses which, at this particular point, dramatically affects overall PA performances.

From EM simulations, each transformer-based power combiner has an insertion loss of 0.6 dB resulting in a total insertion loss of 0.85 dB for the combiner.

The minimum distance between the 4 ways is determined with EM simulations. A minimum distance of 20 μm is necessary to ensure maximum coupling of -20 dB between inductors. The same study was carried out for the power combiner and output stages of the two combined UAs.

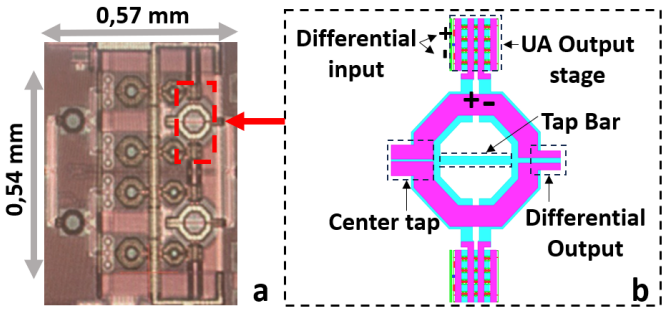

Fig. 2. Chip micrograph of the PA

C. PA stability

The study of PA stability is essential to prevent oscillations, requiring analysis in both large and small signal domains. Large signal analysis checks internal loops stability, defined by gain and phase margins. The stability of each stage of the PA unit was evaluated in simulations in Fig. 3a. For all the studied nodes, the system is stable with a gain margin greater than 10 dB. Small signal stability complements large-signal analysis by examining the overall system stability. A Rollet factor K_f and a geometric stability factor μ greater than 1 ensure the circuit unconditional stability as shown in Fig. 3b.

III. Experimental Results

The chip presented in Fig. 2, was fabricated using a 28 nm CMOS technology. It includes input and output RF pads accessed via GSG probes. Its DC pads are wire-bonded to a Printed Circuit Board (PCB). The PA measurement results presented in Fig. 4 and Table II are compared with 4-way PAs implemented in sub-65 nm CMOS technologies operating in E and V-bands. Among the references, [5] achieves the best gain, slightly surpassing ours, but consumes 510 mW, while [7] reports the highest Psat of 23.7 dBm at the expense of a very large chip area of 0.653 mm². In contrast, our work achieves the best PAE_{max} among all the references, with a smaller chip area compared to [5], [7] and [11]. Although [6] consumes less power, it underperforms in both gain and PAE. The recent design in [10] is compact but shows reduced gain and PAE compared to ours. Additionally, [4] presents good P_{sat} but with significantly higher power consumption and lower gain. As in Fig. 4, measurements are very close to simulations.

IV. Conclusions

This paper details a 4-way PA implemented in 28 nm CMOS technology, featuring a power combiner, splitter, and four amplification units, each containing an NCA stage for relaxing the input power requirements followed by two NCS stages to optimize efficiency. This architecture achieves a PAE of 23 %, the highest among similar PAs operating above 60 GHz. The PA provides a maximum gain of 30 dB and a Psat of 17 dBm, while maintaining low power consumption (194 mW) and a compact die size (0.31 mm²).

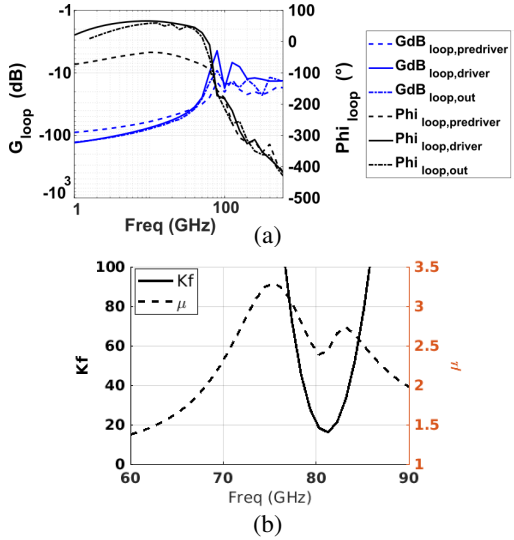

Fig. 3. PA stability for (a) large signal (b) small signal

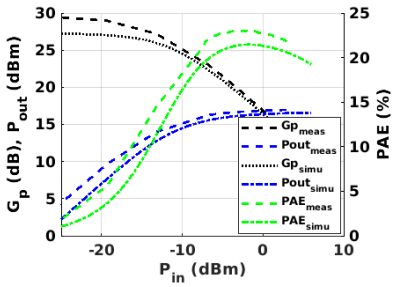

Fig. 4. Measured and simulated performances of the proposed PA at 79 GHz

TABLE II
CMOS PA PERFORMANCES AND COMPARISON WITH THE STATE-OF-THE-ART

	Our work	**[6]**	**[7]**	**[5]**	**[11]**	**[10]**	**[4]**
Freq (GHz)	79	73	60	60	60	77	80
Tech (nm)	28	40	65	65	65	40	40
Psat (dBm)	17	22.6	23.7	19.9	19.7	20.2	20.9
P1db(dBm)	10	18.9	19.9	17.2	16	16.9	17.8
$PAE_{max}(\%)$	23	19.3	22.1	20	13.4	18	22.3
G (dB)	30	25.3	29.7	32.4	28	12	18
Vdd (V)	1.5	1.8	N.A	1.2	1.4	1.1	0.9
Pdc (mW)	194	182	235	510	NA	NA	375
Area(mm²)	0.31**	0.25*	0.65**	0.32**	0.32**	0.152**	0.19*
Topologies	NCA+ 2NCS 4way	2NBCA 4way	2NCS+ 1NCA 4way	NCS 4way	CS+ ISD 4way	2 NCS 4way	2CS 4way

*:with pads; **:without pads

References

[1] C.-W. Wu, et al., "Design of a 60-GHz high-output power stacked-FET power amplifier using transformer-based voltage-type power combining in 65-nm CMOS," IEEE Trans. Microw. Theory Techn., vol. 66, no. 10, pp. 4595–4607, Oct. 2018.

[2] B. Leite, E. Kerhervé and D. Belot, "Design of 28 nm CMOS integrated transformers for a 60 GHz power amplifier," 2015 28th Symposium on Integrated Circuits and Systems Design (SBCCI), Salvador, Brazil, 2015, pp. 1-6.

[3] C.-F. Chou, et al., "Design of a V-band 20-dBm wideband power amplifier using transformer-based radial power combining in 90-nm CMOS," IEEE Trans. Microw. Theory Techn., vol. 64, no. 12, pp. 4545–4560, Dec. 2016.

[4] D. Zhao and P. Reynaert, "An E-Band Power Amplifier With Broadband Parallel-Series Power Combiner in 40-nm CMOS," in IEEE Trans. on Microwave Theory and Techn., vol. 63, no. 2, pp. 683-690, Feb. 2015.

[5] A. Larie et al., "A 1.2V 20 dBm 60 GHz power amplifier with 32.4 dB Gain and 20 % Peak PAE in 65nm CMOS," European Solid State Circuits Conference, Venice, Italy, 2014, pp. 175-178.

[6] D. Zhao and P. Reynaert, "A 40-nm CMOS E-Band 4-Way Power Amplifier With Neutralized Bootstrapped Cascode Amplifier and Optimum Passive Circuits," in IEEE Trans. on Microwave Theory and Techn, vol. 63, no. 12, pp. 4083-4089, Dec. 2015.

[7] Y. Chang et al., "A V-Band Power Amplifier With 23.7-dBm Output Power, 22.1 % PAE, and 29.7-dB Gain in 65-nm CMOS Technology," in IEEE Trans. on Microwave Theory and Techn., vol. 67, no. 11, pp. 4418-4426, Nov. 2019.

[8] J. Kühn, AlGaN/GaN-HEMT power amplifiers with optimized power-added efficiency for X-band applications. Karlsruhe: KIT Scientific Publishing, 2011.

[9] A. -L. Franc, et al., "A Lossy Circuit Model Based on Physical Interpretation for Integrated Shielded Slow-Wave CMOS Coplanar Waveguide Structures," in IEEE Transactions on Microwave Theory and Techniques, vol. 61, no. 2, pp. 754-763, Feb. 2013.

[10] C. Yang, X. Liu, W. Tao, Y. Guo and J. Jin, "A 77 GHz 4-Way Power Amplifier with 20.2 dBm Output Power in 40 nm CMOS," 2022 IEEE MTT-S International Wireless Symposium (IWS), Harbin, China, 2022, pp. 1-3, doi: 10.1109/IWS55252.2022.9977554.

[11] J. -A. Han, et al., "A 26.8 dB Gain 19.7 dBm CMOS Power Amplifier Using 4-way Hybrid Coupling Combiner," in IEEE Microwave and Wireless Components Letters, vol. 25, no. 1, pp. 43-45, Jan. 2015.