An Integrated Miniaturized VNA for On-Chip PA Mismatch Measurement

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Oumayma Belkhadra[1,2], Gilles Montoriol[1], Emmanuel Pistono[2], Hugo Vallee[1], Florent Cilici[1], Manuel J. Barragan[2], Salvador Mir[2] and Sylvain Bourdel[2]
[1]*NXP SEMICONDUCTORS, Toulouse, France*
[2]*Univ. Grenoble Alpes, CNRS, Grenoble-INP, TIMA*

***Abstract*—This paper presents an embedded reflectometer for power amplifier output mismatch measurement. The proposed system is implemented in 28-nm CMOS technology. It consists of two back-to-back directional couplers, two mixers for incident and reflected signal measurements, and finally two Peak Power Detectors for peak voltage measurement. Simulations reveal very good accuracy, with magnitude and phase errors below 0.29 dB and 1.6° respectively, while maintaining a compact area of 0.85 mm^2 with a power consumption of only 3 mW.**

***Index Terms*—VNA, power amplifiers, mismatch, dual directional couplers, reflectometer, peak power detector**

I. Introduction

In the domain of advanced technologies, ensuring seamless integration of electronic components is paramount. However, one challenge lies in mitigating performance degradation due to unavoidable imperfections. In the case of Power Amplifiers (PAs), performance degradation can arise with process variations during the die manufacturing, with packaging issues, aging or inappropriate configuration, such as when the antenna couples with undesirable metallic objects. Those issues directly affect the PA matching, which needs to be continually and accurately monitored in order to apply suitable corrections. Achieving this level of accuracy requires measurements at internal nodes, a complicated task within integrated circuits.

PA systems employ two measurement approaches: scalar and vectorial. The scalar technique measures the magnitude signal using a Peak Power Detector (PPD) [8], logarithmic power detectors [18], RMS power detectors [19], or a coupler with meander line [20]. Another more sophisticated approach studied by [7], involves a directional coupler for coupled and isolated signal measurement, allowing power detection even in the presence of antenna load fluctuations at the PA output. In the same context, six-port architectures are presented in [1]–[4] and multiprobe reflectometers are introduced in [5] and [6]. Despite its good accuracy, this method lacks information on the incident and reflected signal phase. In addition, the main drawback of those architectures is the limited dynamic range (DR) of the used power detectors, which makes it unsuitable for most applications.

To overcome this hurdle, a second approach based on vectorial measurement using mixers has been introduced. [21] [22] studied a transformer with sense winding for current detection and a capacitive divider for voltage measurement. [9] proposed directional bridges for splitting the signal from the Device Under Test (DUT) into incident and reflected waves, while [10]–[13] investigated directional couplers, characterized by their lower losses and highest directivity compared to resistive couplers.

Several studies have been carried out on integrated Vectors Network Analyzers (VNA) for biomedical applications. Few have focused on BIST (Built-In Self-Test) applications. Thus, [9] presents a reflectometer operating in the 0.01-26GHz band, composed of a resistive coupler, and two heterodyne receivers. Its comparison with a commercial VNA shows a small difference of 0.2° in phase and 0.2 dB in amplitude. However, this reflectometer consumes a fairly high power of 640 mW due to the use of amplifiers in the heterodyne receivers. In the same context and using the same technology, [13] developed a reflectometer that is competitive in terms of power consumption and dynamic range, at the expense of the space occupied. A more recent study [10] aims at integrating systems for measuring DUT S-parameters in 55nm SiGE BICMOS technology. It represents the most optimal method in terms of power consumption and space occupied compared with the state of the art of reflectometers operating between 1 and 200 GHz.

In our work, we will focus on the design of an integrated VNA for output mismatch measurement of a PA working at 80 GHz. The proposed reflectometer has a phase and a magnitude error of 1.6° and 0.29 dB respectively. Those values represent the maximum errors for the worst case, which correspond to a reflection coefficient magnitude of 1. The reflectometer has a promising dynamic range of 107dB, which allows very low signal level measurement. In section II, the mismatch measurement principle is explained. Section III describes the VNA architecture design. The results, based on Post Layout Simulations (PLS) are presented in Section IV. Finally, conclusion and directions of further work are given in section V.

II. Mismatch measurement principle

To measure the PA output mismatch, a dual directional coupler (DDC) is integrated on chip. It consists of two back-to-back directional couplers, two passive mixers and finally two PPDs allowing to relax the design constraints on the mixer and serve as validation technique for assessing the reflection coefficient magnitude, as illustrated in Fig. 1.

The directional couplers separate the incident and reflected signals. Through its directional couplers, the reflectometer

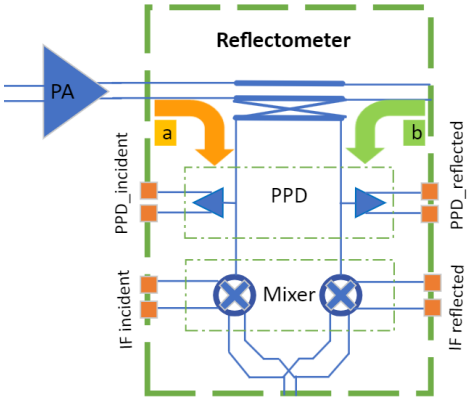

Fig. 1: Bloc diagram of the dual directional coupler

measures incident and reflected power, enabling the value of the reflection coefficient to be determined. Given the non-ideality of these couplers, they tend to introduce phase and magnitude distortion on the reflection coefficient magnitude and phase measurement. As explained in the theory of VNAs [14], there are three error types: systematic, random and drift errors. Systematic errors, which represent the largest contributor to measurement uncertainty, denote predictable imperfections in either the test equipment or the test setup which can be alleviated with calibration process. The most common example of systematic errors is the power loss generated by all the circuitry between the DUT and the VNA outputs. Random errors that are caused by noise from either the test equipment or the test setup will remain in measured results even after calibration. Finally drift errors, which refer to shifts in measurements over time, occur following the completion of a user calibration.

The voltage at the load level can be expressed using (1).

$$V_L = V_L^+ + V_L^- \tag{1}$$

where V_L^+ is the incident wave and V_L^- is the reflective wave. Ignoring the non-idealities caused by the reflectometer, the reflection coefficient can be calculated as follows:

$$\Gamma = \frac{V_L^-}{V_L^+} = |\Gamma| exp^{j\phi_{ref}}, \tag{2}$$

where ϕ_{ref} denotes the reflection coefficient phase in the absence of any non-idealities in the couplers. Fig. 2 illustrates the phase shifts incurred along the path from the amplifier's output to the incident and reflected signals of the real reflectometer.

The measured reflection coefficient phase formula can be derived as follows:

$$\phi_{\Gamma_M} = \phi_{M_{ref}} - \phi_{M_{coup}} \tag{3}$$

$$\phi_{\Gamma_M} = \Delta_{\phi_{coup}} + \phi_{ref} \tag{4}$$

Equation (4) represents the theoretical formula of the reflection coefficient phase error to be compensated. For this purpose, the calibration routine based on the equation presented in [16] [5] is used.

A. One-port calibration mechanism

The calibration routine used is based on the "open", "short" and "load" (OSL) standards as explained in [15]. The measured reflection coefficient can then be linked to the calibrated one using (5)

$$\Gamma_M = e_{00} + \left(\frac{e_{10}e_{01}}{1 - e_{11}\Gamma_A}\right)\Gamma_A \tag{5}$$

$$\Gamma_A = \frac{\Gamma_M - e_{00}}{\Gamma_M e_{11} - \Delta_e} \tag{6}$$

$$\Delta_e = e_{00}e_{11} - e_{10}e_{01}, \tag{7}$$

where e_{00}, e_{11} and Δ_e are the error coefficients, Γ_M is the measured reflection coefficient, and Γ_A represents the calibrated one. For in-depth details on error coefficients calculation, the reader is referred to [15] [16].

B. Output impedance calculus

Upon calibration of the measured gamma, the load impedance at the DUT output is deduced by relying on (8).

$$Z_{M_{cal}} = 50\left(\frac{1+\Gamma_A}{1-\Gamma_A}\right) \tag{8}$$

The error criteria on the calibration routine is defined by (9).

$$\Gamma_e = dB20\left|\frac{Z_{M_{cal}} - Z_{load_{cal}}}{Z_{M_{cal}} + Z_{load_{cal}}^*}\right| \tag{9}$$

where $Z_{load_{cal}}$ is the output impedance applied by the impedance tuner.

III. Reflectometer Design

The dual directional coupler has low insertion losses of 0.9 dB, a reverse isolation of 30 dB, a coupling coefficient of 13 dB and a directivity of 20 dB.

A. Power divider

To route the mixer Local Oscillator (LO) signal through the Ground-Signal-Ground (GSG) pads, a balun initially converts the single-ended signal into differential. Subsequently, differential transmission lines based power divider are deployed to distribute the Local Oscillator (LO) signal between the passive mixers of both the incident and reflected paths.

The power divider converts 50 Ω to the input impedance of each mixer (132-j38) Ω. The insertion loss of the transmission

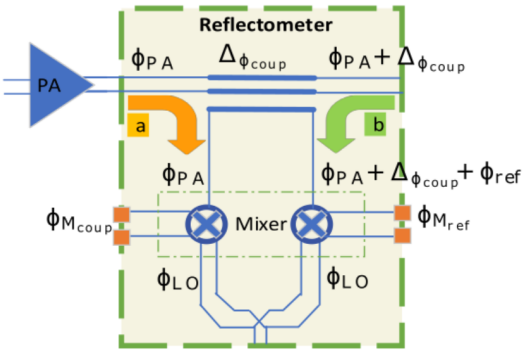

Fig. 2: Phase shifts along the reflectometer

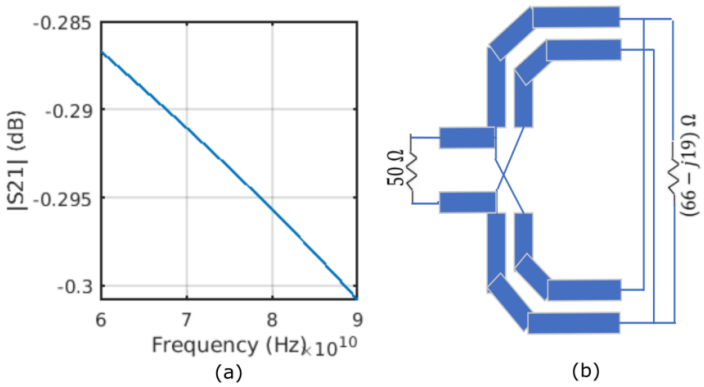

Fig. 3: Power divider: (a) Insertion loss (dB), (b) Schematic

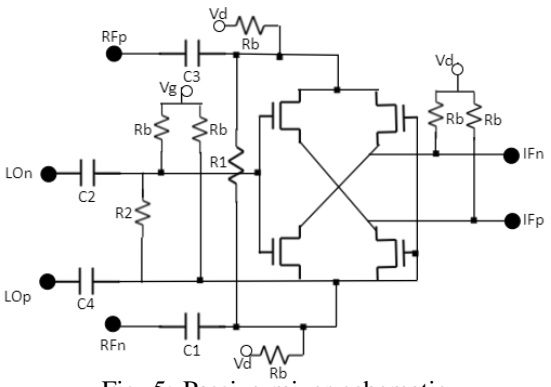

Fig. 5: Passive mixer schematic

lines based power divider is simulated, using a 2.5 D simulator and 2-port setup as illustrated in Fig. 3-(b). This simplification into a standard 2-port circuit assumes identical parallel paths, resulting in the equivalent impedance being half of the value at the input of the mixer. As depicted in Fig. 3-(a), the power divider has an insertion loss of 0.3 dB.

B. Power detector design

Two power detectors are integrated into the chip, one for detecting the incident signal, and the other for the reflected one. They are peak power detectors composed of a diode, a capacitor and a resistor as depicted in Fig. 4. The diode is reverse biased. Therefore, it is conducting half of the time. The signal is redressed by the diodes, then retrieved at an RC low pass filter. A capacitor of $C = 35$ fF help smoothing the rectified signal to obtain a more stable measurement of peak voltage. It eliminates unwanted rapid fluctuations, resulting in a more consistent and accurate output. The detectors illustrated in Fig. 4 have a power consumption of 0.3 mW.

C. Passive mixer

The used mixer is a passive type differential double-balanced rectifier illustrated in Fig. 5. It is characterized by a good linearity, low flicker noise $1/f$, and a negligible power consumption compared to active mixers. The mixer consists of 4-NMOS switches driven by local oscillator signals. The drain D_p and D_n receive the RF signal, the transistor's gates G_p and G_n are driven by the LO signal, while the Intermediate Frequency (IF) signal is retrieved from the source. At the input of the mixer, DC block is ensured by an integrated transformer

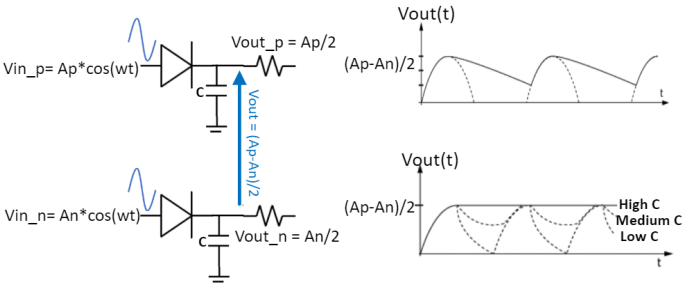

Fig. 4: Peak Power Detector schematic

used for interstage matching between the directional coupler and the mixer. Although resistors R1 and R2 reduce the voltage swing, they aid in achieving power matching at the mixer input, a task that proves challenging due to the capacitive nature of the mixer's input impedance. It also helps improving the RF-LO isolation.

The input LO power was chosen based on both the conversion loss (10) and noise factor simulations. A high LO power reduces the noise factor, and guarantees a linear operation of the mixer. This helps better controlling the switches and finally increases the dynamic of reflectometer. Simulations have demonstrated that the optimum LO power for minimum noise is between 10 and 14 dBm. The LO power was set to 10 dBm due to the power equipment limitation. An Intermediate Frequency (IF) of 100 KHz was chosen.

$$Conversion_{Loss} = \frac{V_{ifRMS}}{V_{RFRMS}} \tag{10}$$

To improve linearity and conversion gain both V_D and V_G are biased as shown in Fig. 5. As illustrated in Fig. 6, where the conversion gain is plotted accordingly with the input power for different V_D and V_G, it appears that exceeding $V_G = 0.75$ V deteriorates both linearity and conversion loss. On the other hand, as long as the drain bias voltage is less than 0.5 V, the input power at 1 dB compression point (ICP-1dB) remains unchanged in Fig. 6-a. However, beyond this bias voltage, linearity deteriorates. Taking this various limitations into account, V_G and V_D of 0.7 V and 0.5 V, respectively, were chosen. The mixer ended up with a conversion loss of 4.5 dB at an ICP-1dB of -1 dBm. One of the main metrics of the mixer is its dynamic range as expressed in (11)

$$DR(dB) = P_{signal}(dBm) - P_{noise}(dBm) \tag{11}$$

where P_{signal} is the ICP-1dB that defines the signal level above which the mixer generates intermodulation distorsion, and P_{noise} is the noise level. The simulated DR is 107dB.

IV. Results

A. Simulation results

To verify the calibration method's accuracy, load pull simulations were performed. The idea is to check that the calibrated

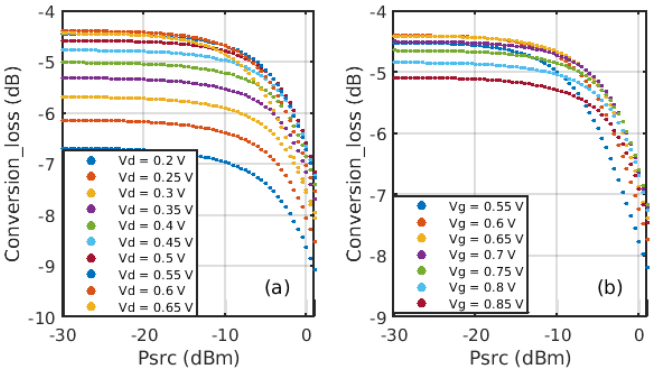

Fig. 6: Conversion loss: (a) for V_G = 0.73V and different V_D values, (b) for V_D = 0.5 V and different V_G values

gamma (Γ_A) is accurate for all load impedances applied to the circuit output. The reflection coefficients before and after calibration are illustrated in Fig. 7 for an applied reflection coefficient magnitude $|\Gamma_{load}| = 1$.

The accuracy of the reflectometer calibration's method is deduced from Fig. 8. The maximum magnitude error between the calibrated reflection coefficient and the targeted one is 0.29 dB, with a maximum phase error of 1.6°.

The accuracy on the load impedance calibration is estimated using the error criteria in (9). As shown in Fig. 9, Γ_e is below -20 dB which endorses the calibration methodology.

B. Comparison to the state of the art

Table I compares our study with prior investigations on the reflectometer. Among all the references, [11] [17] achieve the best magnitude and phase errors respectively, at the expense of a very large chip area of 16 mm^2 and 12 mm^2, respectively. In contrast, our work achieves good magnitude accuracy with a smaller chip area compared to all the other references. Notably, the phase and magnitude error accuracies for our work are presented in Table I for the worst case, which corresponds to $|\Gamma_{load}| = 1$. For the same operating frequency, the proposed reflectometer has the best dynamic range compared to [17].

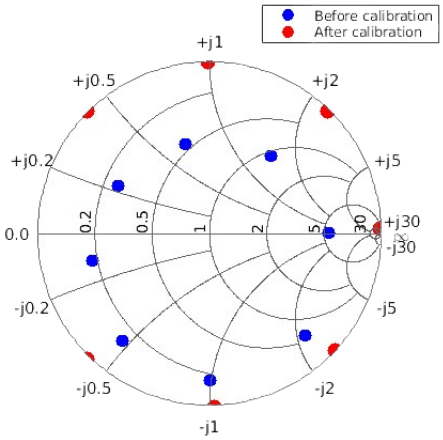

Fig. 7: Reflection coefficient for $|\Gamma_{load}| = 1$ before and after calibration

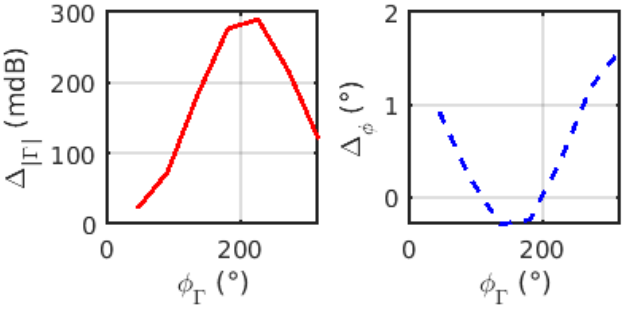

Fig. 8: Error accuracies on magnitude and phase

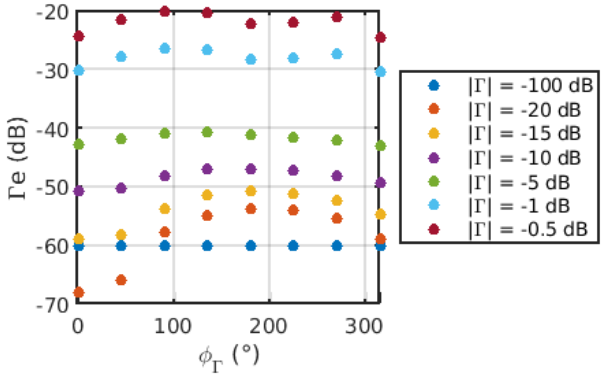

Fig. 9: Accuracy on PA output mismatch value

The power consumption comparison can be misleading since [9] is using cascode RF amplifiers to provide the adequate gain needed by the mixer and IF amplifiers to deliver the appropriate voltage to the Analog Digital Converter. [11] and [17] are employing frequency synthesizer modules with wideband Low Noise Amplifiers. Finally, [10] incorporates G-band integrated quadruplers.

TABLE I: Reflectometer performances and comparison with the state-of-the-art

Reference		our work	[9]	[11]	[10]	[17]
Bandwidth (Hz)		60-90 G	0.01–26 G	4–32 G	172-192 G	50–100 G
IF Freq (Hz)		100 k	10	100 k	10 M	100 k
Tech (nm)		28 CMOS	SiGe	0.35um SiGe	55nm BiC-MOS	0.35um SiGe
Vsupply (V)		0.9-1.45	3.3	3.3	1.2	3.3
Calibration type		3-term	12-term	16-term	3-term	12-term
Area(mm^2)		0.85	1.8	16	3.3	12
Accuracy	mag(dB)	< 0.29	0.6	0.17	0.3	0.3
	phase(°)	< 1.6	5	1.3	NA	0.3
Dynamic Range(dB)		107+-2	129+-3	82-101	NA	56-72
Component for detection		Passive mixer	Passive mixer	Micro-mixer	Passive mixer	Mixer

V. Conclusion

This paper deals with an integrated VNA implemented in 28-nm CMOS technology, for PA output mismatch measurement. The reflectometer incorporates two back-to-back directional couplers, two PPDs and two passive mixers. Despite its low dynamic range, the PPD has been integrated on chip to alleviate the mixer design constraints that are related to its 1-dB compression point. To eliminate the non-idealities of the reflectometer, a calibration routine has been investigated based on OSL standards. The post-layout simulations show good

magnitude and phase accuracies, with promising dynamic range compared to the state of the art. As we move forward, this method will be implemented in BIST applications, shaping the future directions of our research.

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