Zero-Overhead Nonintrusive Test of mmW Integrated Circuits Based on Wafer-Level Parametric Tests

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***Abstract*— This article presents a nonintrusive integrated test methodology based on machine learning for predicting the performance of millimeter-wave integrated circuits solely from measurements of Parametric Test sensor signatures (quasi-static and automated wafer-level measurements). These sensors are designed and integrated by the foundry to monitor process variations and are inherently non-intrusive and generic. The test method was applied to a 25 GHz Low-Noise Amplifier in a 55-nm BiCMOS technology. Experimental results on a set of 57 fabricated devices demonstrate the ability of the method for predicting the gain and NF of the LNA from Parametric Test signatures with an RMS error below 0.07 dB and 0.014 dB, respectively.**

I. INTRODUCTION

Since the early 2000s, there has been a growing trend in millimeter-wave (mm-wave) applications for System-on-Chip (SoC) systems in multiple domains. Emerging applications include high-resolution automotive radar or high-data-rate communications, with the nowadays well-established 5G and its developments in the K- and Ka-bands. In the medium term, it is estimated that 6G will expand up to the D-band (110 – 170 GHz) for backhauling.

Thus, for these applications, the front-end is a critical circuit whose performance constrains the entire system operation. At the same time, the increasing operating frequencies require regular technological innovations, which simultaneously reduce the technological node dimensions and increase the circuit's sensitivity to process variations. Furthermore, the widespread adoption of applications at mm-waves requires the production of large volumes of front-ends. Testing these circuits becomes crucial, and direct measurement (functional test) is often costly. This test requires specific benches for analog and RF/mm-wave characterization, time-consuming measurements, and expensive automated test equipment.

Various approaches have been proposed in the literature to reduce test complexity and cost. Firstly, the use of structural testing as used for digital circuits can be discussed as a potential solution. However, it does not seem to be a reliable method for testing analog circuits due to the challenges in developing and simulating a complete fault model [1].

As a first improvement, reduction of the measurement complexity has been addressed by using indirect test, often called alternate test in the literature [2]: instead of measuring the performance of the device-under-test (DUT), a sensor is added to the DUT to give a response, i.e., a signature, correlated to the performance to test. In these built-in test methods, these signatures can be generated from multiple sources, for instance from built-in power detectors, current detectors [3], monitoring DC node voltages [4], time-domain response to an optimized stimulus [2], the oscillation characteristics of an oscillation-based test (OBT) as in [5], etc. In these methods, the relation between sensors signature and the performance to predict is obtained by statistical treatment or machine learning on a set of empirical data. However, even with a good test quality and low-cost measurements, this approach presents some disadvantages: (i) the sensors load the DUT and might cause additional loss for mm-wave devices, (ii) this addition leads to heavy co-simulation needs during the design step, (iii) the method is not generic, the test has to be effectively redefined for each new DUT.

Partial solutions to these drawbacks have been explored in the context of nonintrusive alternate test [6], [7], [8], [9]. This methodology allows separating the sensors from the DUT: sensors target the measurement of technological process variations independently of the DUT itself. As long as the sensors signatures are correlated to the DUT performance, i.e., if sensors and performances are sensitive to the same process variations, a regression model can be built to predict the DUT performance from the nonintrusive signatures. Thus, non-intrusive sensors are usable, and remove the risk of performance degradation of the DUT and the co-design requirements. Nevertheless, the design of new sensors for each new DUT is needed most of the time (even if generic methodologies for nonintrusive sensor design have been presented [8]), and this method leads to a significant silicon overhead, since each sensor is independent from the DUT and hence requires additional area.

In this article, we propose a method that tackles this challenge by using the Parametric Test (PT) sensors integrated by the foundry as a new kind of non-intrusive process variation sensor. These PT sensors are process variations sensors integrated by the foundry at wafer-level on the cutting paths of each die to monitor the technology, in order to monitor the technological corners of each wafer for the designer/customer. These sensors are designed to ensure that all the relevant process parameters are monitored, and to be easily measured with quasi-static analog Automated Test Equipment (ATE). Additionally, as they are placed in the wafer cutting paths, they do not incur in area overhead.

In this paper, we propose a non-intrusive test methodology that utilizes these PT sensors already available in a given technological process to predict the performance of a mm-wave circuit. This assumes that among the population of PT sensors, we will be able to identify a subset of signatures strongly correlated to the performance of the DUT, in such a way that we can build a regression function that predicts mm-wave DUT's performance using only PT signatures. Thus, this

method is non-intrusive, fully generic (as PT sensors monitor the process variations, not the DUT), without any silicon overhead, and relying on fully automated quasi-static measurements already routinely performed by the foundry at no extra cost.

As a case study to demonstrate the proposed methodology, we consider a Low Noise Amplifier (LNA) designed using STMicroelectronics 55-nm BiCMOS technology. The LNA is positioned at the input of the reception chain and is critical as its own performance significantly impacts the entire reception chain. The LNA test is particularly interesting as its noise characterization is challenging, and the method ultimately aims to overcome this constraint in production.

The paper is organized as follows. In section II, we introduce some alternate nonintrusive methods discussed in the literature, then we present our proposed test methodology based on PT sensors. Section III describes the case-study, with a short presentation of the 25 GHz LNA under-test and the set of PT sensors integrated on STMicroelectronics 55-nm BiCMOS technology. In section IV, we discuss the results of the test and the performance prediction. Finally, section V summarizes the main contributions of this work.

II. Proposed Methodology

A. Non-intrusive and Alternate Test overview

The first approach to nonintrusive test was introduced by [6], and applied to the test of an ADC. Non-intrusive sensors around the DUT are based on stand-alone components from the DUT. They are measured by integrated test blocks and all the sensors are accessible through a multiplexer. The Go/NoGo decision (i.e., the decision to accept the chip as its performance is in accordance with the specifications)is taken directly on the chip, by a dedicated logic circuit, and the information is transmitted digitally to an external ATE. In this way, the authors of [6] introduce a fully automated method based on non-intrusive sensors. On the first hand, the test is drastically simplified, but on the other, the design complexity is increased, with the integration of a full digital circuit dedicated to the computation of the decision, with a 10% silicon overhead. Furthermore, the relation between the performance of the DUT and the sensors signatures was determined formerly with an analytical model. Thus, the process variation sensors and their relation with the performance of the DUT are specific to this ADC.

To ease the sensor design and the determination of the relation between sensors signatures and performance, an alternate test strategy was adopted [7, 8]. It relies only on the fact that process variation sensors signatures are correlated to the performance that we want to predict. The alternative test method is composed by two main steps, as depicted in Figure 1.

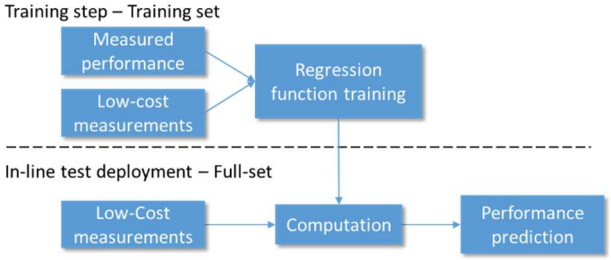

Fig. 1. Principle of alternative test

Firstly, a training set is gathered, composed by low-cost measurements (the sensors signatures) and their corresponding DUT performance functional measurement. A regression function is trained, in order to predict the performance from the signatures. Secondly, the regression function is deployed to the test step. During the test, only the sensors signatures are measured with an ATE, and we can predict the DUT performance through the regression function. A Go/NoGo decision is then taken with regard to the specifications' test limits.

Several developments of this nonintrusive alternate test have been described in the literature. It has been applied for RF on a 2.4 GHz LNA integrated on 0.25 µm Qubic4+ BiCMOS in [7]. In this study, authors add various sensors in the immediate proximity of the DUT, most with topologies very similar to the DUT stages (e.g. power supply stage identical to that of the LNA, current mirror, cascode stage). These sensors are located as close as possible to the LNA to prevent any intra-die variation effect from biasing the obtained results. After a training step based on measurements, performance (Gain, Noise Figure - NF, 1-dB Compression Point – 1-dB CP, and Third-order Intercept Point - IIP3) are predicted with a worst mean error of ε_m = 2.2 % on the 1-dB CP on the overall performance. The proposed sensors are stand-alone parts of the DUT, but no methodology is identified to provide appropriate sensors for a generic DUT. To address this issue, the authors in [8] propose a generic methodology for designing a set of simple process variation sensors allowing to provide all the necessary observations to predict a given performance for a given, arbitrary, DUT. The sensor set is built from the simulation step: (i) Monte-Carlo (MC) simulations of the DUT are done with Process Design Kit (PDK) models, simulating process variations through MC parameters, (ii) MC parameters that are most correlated to the performance of the DUT are selected, (iii) low-cost sensors are designed for signatures with a strong correlation to the selected MC parameters. This solution permits to achieve a good genericity, after the application on several kinds of DUT. Next, reference [8] indirectly proposes to focus more on monitoring the process variation involving the performance variations than testing the performance variation itself.

In this paper we intend to push this strategy a step further. By taking advantage of the wafer-level technological characterization databases, that already contain the process variations of all the relevant technological parameters identified by the foundry, it would be theoretically possible to predict the behavior of a given DUT, the challenge being to identify the relevant information in this database.

In this regard, we propose a methodology to predict RF/mm-wave DUT performance with PT data only. Using only PT data for the test reduces the complexity of the test because (i) no sensor is added to the die (zero silicon overhead); (ii) no additional design is needed from the DUT designer; (iii) measurements are optimized by the foundry to stay below a tenth of kHz with an ATE; (iv) PT sensors give information on the relevant parameters of the process, and are consequently fully generic; (v) and as the performance is correlated to the process whatever the frequency, the prediction is theoretically not frequency-limited.

B. Process Variation and Parametric Test Sensors

To monitor parametric process variations, the full set of PT sensors is embedded around each die or chip, into the

scribe line, so in a lost silicon area. Each die includes a complete set of sensors, allowing precise inter-die variations characterization. Usually, a process corner validation of each wafer is tested by measuring a certain number of full set of PT across the wafer. A Go/NoGo decision is taken from this result at the wafer-level. Statistics from PT measurements on the production line are also directly integrated into the PDK for modeling MC models. In an advanced technology, such as the selected STMicroelectronics BiCMOS 55 nm technology, the set of PT signatures per die contains more than a thousand measurements.

Although we cannot disclose the topology of the PT sensors designed by STMicroelectronics, we can point out that PT sensors have been optimized to be measured in DC or quasi-static conditions, providing voltage or current mode measurements. The PT sensors are composed by passive and active cells from the PDK and specific test structures optimized for monitoring particular technological metrics.

As it should be clear, the complete set of PT signatures would not be relevant for the test of a specific DUT. Only a subset of PT measurements would be actually correlated to the DUT performance. The most relevant PT signatures will be selected during the training step to optimize the prediction performance and reduce the measurement time. Trying to employ the complete set of PT measurements for performance prediction would severely hinder the quality of the predicting model, since all non-relevant signatures would just add unwanted noise to the model training.

C. Methodology

In essence, the proposed test methodology is a classical alternate test strategy that follows the principle described in Figure 1. As a selection of relevant PT signatures is needed, feature selection has to be performed before the training step. A data set with the DUT performance and the identified relevant PT signatures is measured for the training step. This set is employed to build a regression function, in our case a perceptron neural network, as,

$$f_{S\to P} : (S_1, S_2 \dots S_n) \to (P_1, P_2 \dots P_m) \qquad (1)$$

where $(P_1, P_2 \dots P_m)$ are the performances of the DUT, and $(S_1, S_2 \dots S_n)$ the PT signatures.

Defining the appropriate input space, that is, the relevant PT signatures, is a key point of the proposed methodology. In this work we employed a feature selection algorithm based on a guided search in the signature space [10]. The search algorithm proceeds as follows. First, we select the signature S_i that has the highest correlation with target performance P_i. As the relation between S signatures and P performances can be nonlinear, the conventionally used Pearson coefficient is not sufficient to identify the most relevant signatures. Brownian distance correlation, as described in [11], is more efficient for this application. A first regression function $f_{S\to P}$ is trained with the training set using the selected signature S_i. Next, we compute the residue of prediction (i.e., the difference between the predicted value and the actual value of the performance) on the verification set. Then, we compute the Brownian distance correlation between the residues and the remaining signatures, and select the most correlated one as the next signature to be added to the input space. The process is then iterated. Conceptually, in each iteration, the algorithm adds the signature that better explains the prediction error obtained in the previous iteration. When the prediction error goes below a predefined threshold, the algorithm stops and outputs the set of identified relevant signatures and a regression function $f_{S\to P}$. Finally, in the test phase, the obtained regression function is deployed on the production samples. During the test phase, only the selected PT sensors have to be measured, while the DUT performance is predicted from the selected PT sensors readings (i.e., the relevant signatures).

III. Case Study : 25-GHz LNA

A. 25-GHz HBT LNA Design

A Low-Noise Amplifier (LNA) operating at 25 GHz, at the beginning of the mm-wave band, has been designed as a demonstrator on the STMicroelectronics BiCMOS 55-nm technology. The LNA stands out as an interesting DUT due to its substantial impact on the entire reception channel on one hand, as well as the variety of performances to be evaluated (Noise Figure, Gain, matching, ...) on the other hand. Figure 2 depicts the LNA, with component values provided in Table 1. The LNA was built using a HBT cascode configuration. Matching networks were designed with lumped elements (inductance, MOM capacitor), optimized using models provided in the Design Kit, while passive components undergo electromagnetic simulation for further refinement.

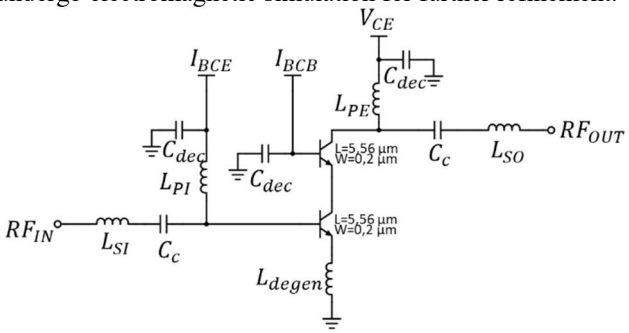

Fig. 2. LNA under-test schematic

TABLE I. Values of Components

Component	Value
C_{dec}	3 pF
C_c	1.14 pF
L_{degen}	70 pH
L_{SI}	330 pH
L_{PI}	890 pH
L_{PO}	460 pH
L_{SO}	950 pH

TABLE II. LNA Measured and Simulated Performance

Performance	Simulated	Measured
Frequency (GHz)	25	25
-3 dB RBW (%)	42%	44%
Gain (dB)	11	10.8
NF (dB)	1.9 – 2.2	2.41 – 3.09
OCP1dB (dBm)	-3.5	-1.3
PDC (mW)	12.2	12
Area (w/o pads) (mm²)		0.093

The LNA biasing was done through three DC pads, one base current for each transistor (I_{BCE} et I_{BCB}), and one voltage supply (V_{CE}). Schematic and electromagnetic (for passive devices) simulation and measurements of a single LNA are summarized in Table II.

B. PT sensors

In the selected 55-nm BiCMOS technology, each die integrates more than 1500 PT sensors for BEOL and FEOL (MOS/HBT) monitoring purposes into the scribe lines.

For our demonstration, we had access to a complete wafer, providing a total of 57 reticles. The PT sensors on all samples were measured upstream by the foundry using quasi-static automated analog testers. The 57 fabricated LNAs were characterized using dedicated RF equipment. S-parameters were measured with a PNA E8361A Vector Network Analyser from Keysight, and Noise Figure (NF) was measured with a bench composed of an NFM HP 8970B, with a Down Converter, and the noise source NoiseCom NC346V.

IV. Results

A. Performance prediction

The first step of the proposed methodology is the selection of relevant PT sensors. The available data (57 samples) was divided into a random 25%-75% split for validation and training sets, respectively. The training set is employed for signature selection and training, while the independent validation set is used to quantify the quality of the performance prediction. In this regard, to quantify the prediction error, we use the RMS error, ε_{RMS}, defined as :

$$\varepsilon_{RMS} = \sqrt{\frac{\sum_{i=1}^{n}\left(P_i - \hat{P}_i\right)^2}{n}} \qquad (2)$$

where n is the number of elements in the verification sample, P_i and $\hat{P}_i$ are the actual and predicted performance, respectively.

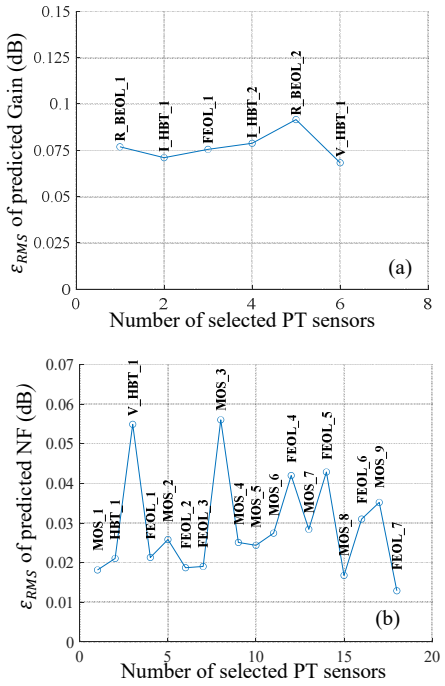

Fig. 3. Evolution of the prediction RMS error for the test set: (a) Gain and (b) NF

In this paper, due to the lack of space, we demonstrate the methodology for the prediction of the LNA gain and noise figure (NF). The methodology can be extended to the rest of the LNA performances. Figure 3(a) and (b) show the evolution of RMS error according to the number of PT sensors selected by the search algorithm, for the gain and the NF, respectively. We can observe that, as the relation between signatures and performances is multivariate, a convenient combination of input signatures is needed to get a good prediction. A total of only 6 PT sensors over the 1500+ sensors were selected to predict the gain of the LNA at 25 GHz and 18 PT sensors to predict the NF, respectively. The selected PT sensors to predict the gain are mainly DC resistance located in the BEOL, and DC current and voltage on HBT devices located in the FEOL. Only 6 quasi-static measurements are necessary to predict the gain with a ε_{RMS} of 1.6% (in linear scale), or 0.068 dB. Figure 4 depicts the prediction of the gain and the NF against their target (i.e., the actual values), for both the training and the verification sets. Finally, Table III summarizes the obtained prediction error for each performance and offers a direct comparison to the dispersion of the functional measurements across the fabricated samples. As can be seen, the prediction error is below the observed variability, which indicates that the prediction function outperforms the naive predictor that simply outputs the average observed value of the performance for all samples, thus validating the proposed approach.

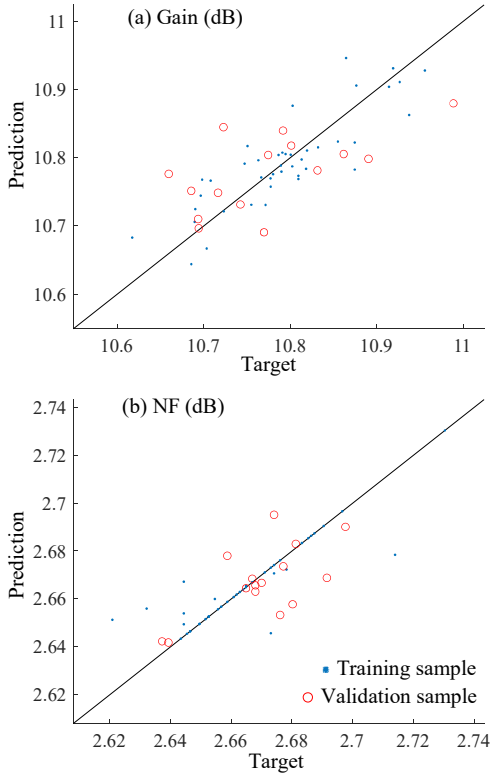

Fig. 4. Prediction of (a) Gain and (b) NF, of the LNA under-test at 25 GHz

TABLE III. Results Summary

Performance	Functionnal measurements			Prediction		
	Min.	Max.	Std σ	ε_{RMS} (dB)	ε_{RMS} (lin. %)	Nb. of selected features
Gain (dB)	10.62	10.95	0.08	0.068	1.6	6
NF (dB)	2.62	2.73	0.02	0.013	0.3	18

V. Conclusion

In this paper, we have proposed a nonintrusive alternate test method that predicts the mm-wave performance of a DUT using only the set of Parametric Test sensors integrated on the wafer by the foundry. These sensors are nonintrusive and are integrated on each die, incurring in zero area overhead on the DUT. Their topology is made and maintained by the founder to be able to monitor the relevant technology process variations with fully automated quasi-static measurements. The application to an LNA operating at 25 GHz has shown that the method can indeed predict mm-wave performances as gain and NF based only on quasi-static wafer-level PT measurements.

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