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Design-oriented single-piece explicit *I*-*V* DC charge-based model for MOS transistors in nanometric technologies

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ABSTRACT This paper proposes a design-oriented DC model for MOS transistors in advanced nanometric technologies, based on only six parameters. The proposed model is based on the inversion charge and includes the main short-channel effects for accurately describing the behavior of the transistor DC drain current in all regions (linear to saturation) and regimes of operation (weak to strong inversion). The proposed model is critically compared to existing inversion charge-based models, highlighting the main limitations of previous models presented in the literature and the advantages and disadvantages of our proposal. Then, regarding the model implementation, previously presented inversion charge-based models require a numerical solver to link the transistor's DC current to its DC node voltages. In this work, we propose an innovative approach to model implementation via the analytical approximation of the Lambert function's principal branch. Thanks to this approximation, the proposed design-oriented model offers for the first time an analytical single-piece expression of the drain current as an explicit function of the transistor node voltages. The validity of both the proposed transistor DC model and its analytical single-piece implementation is confirmed through simulation and measurement results, using the industrial production-level model UTSOI2 as a reference. The evaluations were conducted on MOS transistors with lengths of 30 nm, 60 nm, and 150 nm in STMicroelectronics 28 nm FD-SOI CMOS technology, to validate our results in minimum length, intermediate length, and long transistors in the selected technology. The proposed model achieves an average error of less than 6% in drain current evaluation compared to industry-standard models such as UTSOI2, while significantly reducing computational complexity.

INDEX TERMS ACM, charge-based MOSFET model, design-oriented MOSFET model, EKV, FD-SOI, Lambert *W*-function, MOSFET compact model, short-channel effects.

I. INTRODUCTION

ULTRA-LOW power and ultra-low voltage standards such as those used in IoT force engineers to design circuits within stringent energy consumption constraints. Unlike digital circuitry, that easily benefits from technology scaling, in order to comply to this requirement, analog designers in advanced technologies are forced to move the transistors' operation zone away from strong inversion, towards the moderate and weak inversion regimes [1]. Describing the physical behavior of the transistor in these regimes taking into account the emergence of short-channel effects in advanced nanometric technologies is a challenging endeavor. Simple models like the long-channel strong-inversion approximation are no longer valid and designers have to rely on complex simulation-based transistor models that accurately describe the transistor behavior and computer-based optimization campaigns to appropriately size their circuits. This simulation-based design methodology is lengthy, resource-intensive and makes difficult to gain an intuitive understanding of the link between design performance and transistor parameters.

In order to overcome the issues of simulation-based design methodologies, simplified design methodologies have been proposed such as the g_m/I_D or the inversion coefficient (IC) based methodologies [2] [3] [4] [5] [6] [7] [8] [9] [10]. These design methods propose an efficient design-space exploration based on simplified design-oriented models that approximate the transistor behavior using a reduced set of model parameters. Accurate and simple design-oriented models describing with precision the behavior of the transistor in all operating regions and regimes are then required to make the best use of these design methods.

In this regard, design-oriented inversion charge-based models have been presented in the last few years [11] [12] [13] [14] [15] [16] [17] [18] [19], usually based on the ACM or EKV formalisms. Different implementations of these design-oriented models have been developed with different levels of complexity, from the classical three-parameter model for long-channel transistors presented in [11] to a seven-parameter model considering short-channel effects for advanced technologies in [14]. These models are well-suited for design applications because of their reduced set of parameters and their fully continuous behavior. It should be noted that these models are compatible with all types of transistors based on the MOS technology operation principles. Thus, the ACM model was initially proposed for bulk CMOS transistors [11] and was subsequently extended to SOI transistors [14], [16]. Recent articles, such as [20], demonstrate that a charge-based model can effectively describe the behavior of FinFET transistors, considering specific physical characteristics of FinFETs. However, the drawback of these all-regime all-region models is the lack of an explicit analytical link between the drain current and the transistor node voltages. Indeed, these models express both the transistor's DC drain current and the transistor's node voltages as a function of the normalized inversion charges at the source and drain sides of the transistor. The resulting system of equations defines a set of transcendental equations[1] and requires a numerical solver to finally obtain the transistor's DC drain current for a given set of values of the transistor's node voltages.

Due to the transcendental nature of the model equations, even if the models remain simple, the intuitive link between voltage and current is unfortunately lost behind the use of a numerical solver, which leads again to computation complexity and complicates the understanding of the transistor behavior.

In this paper, we present a single-piece continuous and explicit MOSFET model for advanced technologies. This model, based on the ACM inversion charge formalism, expresses the MOS transistor's drain current as an explicit function of the transistor's node voltages in a closed-form analytical expression valid for all the operation zones of the transistor. Although the ACM formalism is employed in this paper, it should be noticed that the proposed approach is directly applicable to other charge-based models such as EKV. The proposed explicit model is based on a recently proposed approximation of the Lambert W-function [21] that avoids the need of a numerical solver in the model implementation, combined with a new description of the transistor's saturation based on a modification of the Unified Charge Control Model (UCCM) [15], that allow us to express the transistor's drain current as a single-piece equation.

Thus, in a nutshell, in this paper we propose a new design-oriented DC model for MOS transistors in advanced nanometric technologies, based on only six parameters, which accurately captures the main short-channel effects. The model employs an innovative approach to model implementation via the analytical approximation of the Lambert function's principal branch, eliminating the need for numerical solvers. For the first time, we provide an analytical single-piece expression of the drain current as an explicit function of the transistor node voltages, valid for all regions and regimes of operation. The validity of the proposed model and its implementation is confirmed through extensive simulation and measurement results on MOS transistors in STMicroelectronics 28 nm FD-SOI CMOS technology and we critically compare the proposed model to existing inversion charge-based models and industry-standard FD-SOI UTSOI2 model, demonstrating its advantages in terms of accuracy and computational efficiency.

The rest of the paper is structured as follows. Section II presents a new 6-parameter (in the following, 6PM) version of the ACM model including the proposed modification of the UCCM to take into account the saturation effect proposed in [15]. The model is described based on the classical transcendental formalism using the Lambert W-function. Then we discuss the traditional implementation of the model using a numerical solver and its underlying complexity. Then, Section III presents our explicit I-V model, that is built from the 6PM model by employing an analytical approximation of the Lambert W-function. Besides, this approximation is employed to derive new analytical expressions for the transistor's drain current and its derivatives. In order to verify the feasibility and validity of the proposed explicit I-V model, Section IV compares, for different operation conditions (operation regions, long and short channels), the proposed model to previous design-oriented models implemented with numerical solver. The comparison is based on transistors from STMicroelectronics 28nm FD-SOI technology. The accuracy of the approximated explicit expression is validated by comparing the obtained results with a numerical implementation of the proposed 6PM model employing the association for computing machinery (acm) 443 algorithm [22].The proposed model is compared to the industry-standard FD-SOI UTSOI2 model. Additionally, comparisons with measurements are made. Finally, an in-depth analysis of the proposed model and its implementation, as well as a comparison with recent state of the art charge based models are presented in Section V. To conclude the paper, Section VI summarizes our main contributions.

[1] A transcendental equation is an equation that is not algebraic, that is, at least one of its sides contains a transcendental function. A transcendental function, such as the exponential, logarithmic and trigonometric function, in contrast to an algebraic function, cannot be expressed algebraically using a finite amount of terms. Transcendental equations are common in applied mathematics and cannot be solved through simple algebraic manipulations.

II. DESIGN-ORIENTED 6-PARAMETER INVERSION CHARGE-BASED MODEL

The aim of a design-oriented model is to assist designers during the initial stages of circuit design. These models have to be built to offer a good trade-off between the model simplicity and accuracy in such a way that the model remains simple to manipulate while approximating the transistor's behavior as closely as possible. In this regard, the proposed 6PM design-oriented model describes the transistor's DC behavior based on only 6 DC parameters linked to different physical effects.

The proposed 6PM model, presented hereafter, is built on the basis of the ACM formalism [23]. Thus, the model includes the three classical parameters from the basic ACM model: the subthreshold slope factor, n, the equilibrium threshold voltage, V_{T0}, and the specific current, I_{S0}, which are enough to approximate the behavior of a long-channel MOS transistor. Three parameters are added to account for short-channel effects. The first one is the drain-induced barrier lowering (DIBL) effect, which leads to a reduction of the carrier's barrier potential occurring at the source side as the drain voltage increases. This effect is represented in the model by the dimensionless DIBL effect factor, σ, that modulates the threshold voltage depending on the DC voltages applied to the source and drain terminals. The effective mobility of the carriers in the inversion layer is directly linked to the vertical electrical field along the channel. The mobility decreases as the applied electrical field increases, which results in a reduction of the drain current and is represented in the model by the mobility reduction factor, θ. Finally, the carrier velocity saturation effect models the limited increase of the velocity of the carriers when the horizontal electric field increases, which again results in an effective reduction of the drain current. This effect is represented in the model by the carrier velocity saturation effect parameter, ζ. This dimensionless parameter is defined as,

$$\zeta = \frac{\mu U_T}{L} \cdot \frac{1}{\nu_{sat}}, \tag{1}$$

where μ is the effective mobility of the carriers, $U_T = \frac{kT}{q}$ is the thermal voltage, L is the transistor length, and v_{sat} is the saturation velocity of the carriers. The presented parameters are summarized in Table 1.

TABLE 1: Summary of the 6PM model parameters

Symbol	Name
n	Sub-threshold slope factor (-)
V_{T0}	Equilibrium threshold voltage (V)
I_{S0}	Specific current (A)
σ	DIBL effect factor (-)
ζ	Carrier velocity saturation factor (-)
θ	Mobility reduction factor (-)

Concerning the dependence of the model parameters with the transistor geometry, that is, its Length, L, and Width, W, it is important to emphasize that parameters n, V_{T0}, σ, ζ, and θ are influenced exclusively by L. Conversely, parameter I_{S0}, has a dependency on both W and L, although the dependence with W is linear. Consequently, the geometrical dependencies of the inversion charges, the drain current and its derivatives, are directly incorporated into the MOSFET model parameters. In a practical application, the usual modeling approach consists in extracting a different set of model parameters for each of the transistor's lengths considered. Nevertheless, it is also possible to derive geometrical scaling laws that represent the model parameters as a function of the transistor dimensions, as demonstrated in [24].

The main equation in the proposed model describes the behavior of the DC drain current I_D taking into account both drift and diffusion currents as well as the saturation velocity and mobility reduction phenomena. Thus, the normalized drain current, i_D, is expressed as,

$$i_D = \frac{I_D}{I_{S0}} = \frac{(q_S - q_D)(q_S + q_D + 2)}{[1 + \zeta (q_S - q_D)][1 + \theta (q_S + q_D)]}, \tag{2}$$

where I_{S0} is the specific current, and q_S and q_D are the normalized inversion charge densities at the source and drain sides of the transistor, respectively.

The specific current is defined as,

$$I_{S0} = \mu n C'_{ox} \frac{U_T^2}{2} \frac{W}{L_{eff}}, \tag{3}$$

where C'_{ox} is the oxide capacitance per unit area, W is the width of the transistor and L_{eff} is its effective length.

The normalized inversion charge densities are defined as,

$$q_i = \frac{Q_i}{Q_P}, \tag{4}$$

where, Q_i represents a charge density (corresponding to source or drain) and Q_P is the pinch-off charge per unit area defined as

$$Q_P = \pm n C'_{ox} U_T, \tag{5}$$

where the plus sign refers to a p-channel transistor and the minus one indicates an n-channel transistor.

The model equations are completed by the relationship between the normalized inversion charges and the transistor node voltages. These equations are defined by the Unified Charge-Control Model (UCCM). We employ the formalism first introduced in [15] to describe the saturation effect directly in the UCCM equations, as

$$v_P - v_{S(D)B} = q'_{S(D)} - 1 + \ln\left(q'_{S(D)}\right), \tag{6}$$

where drain and source voltages are normalized with respect to U_T and v_P is the normalized pinch-off voltage approximated as,

$$v_P \approx \frac{1}{U_T} \cdot \frac{V_{GB} - V_{T0} + \sigma (V_{DB} + V_{SB})}{n}. \tag{7}$$

Introducing the modulated threshold voltage, defined as

$$V_T = V_{T0} - \sigma (V_{DB} + V_{SB}), \tag{8}$$

(7) can be expressed as,

$$v_P \approx \frac{1}{U_T} \cdot \frac{V_{GB} - V_T}{n}. \tag{9}$$

In order to consider the carrier velocity saturation effect, modulated normalized source and drain inversion charges, q'_S and q'_D, respectively, have been introduced. They are defined as,

$$q'_{S(D)} = q_{S(D)} - q_{sat}, \tag{10}$$

where q_{sat} represents the normalized saturation drain charge ratio and is related to the normalized saturated drain current by

$$i_{Dsat} = \frac{2}{\zeta} q_{sat}. \tag{11}$$

The introduction of q_{sat} in the UCCM equations allows for a continuous description of the transistor behavior across the different operation zones, avoiding the definition of a saturation voltage leading to a piece-wise set of equations and a higher calculation complexity. It is also worth noticing that by modulating both the source and drain inversion charges, the resulting equations are symmetrical, in the sense that interchanging drain and source terminals results in a change of sign of V_{DS} but the transistor behavior remains the same.

Expressions (2) and (6) define a system of equations that determines the value of the transistor's DC drain current as a function of the transistor's DC node voltages. The analytical solution of the system can be written in terms of the Lambert W-function, which is defined as the solution of the transcendental equation (6), as,

$$q'_{S(D)} = W(x_{S(D)}), \tag{12}$$

where,

$$x_{S(D)} = e^{[v_P - v_{S(D)B} + 1]}. \tag{13}$$

The normalized saturation drain charge ratio q_{sat} can then be expressed as

$$q_{sat} = \frac{\zeta}{2}\left[(W(x_S)+1)^2 - 1\right]. \tag{14}$$

Substituting (12) and (14) in (10) leads to,

$$q_{S(D)} = W(x_{S(D)})\left[1 + \frac{\zeta}{2} W(x_{S(D)}) + \zeta\right], \tag{15}$$

which can be introduced in (2) to compute the transistor drain current. It is interesting to note that $\frac{\zeta}{2} W(x_{S(D)}) \ll 1$ when the transistor is not saturated which leads to

$$q_{S(D)} = W(x_{S(D)})\,[1+\zeta] \approx W(x_{S(D)}), \tag{16}$$

and thus to $q'_{S(D)} \approx q_{S(D)}$, which enables to create a link between the modified UCCM used in this paper and the classical one, not taking into account the carrier velocity saturation effect, which is commonly used in the literature.

Due to the transcendental nature of (6), the solution (12) is computed with a numerical solver. This is a common drawback for models based on the UCCM equation. Thus, the classical implementation of these models employs an efficient numerical solver, the acm 443 algorithm, to numerically solve the UCCM equations.

The numerical implementation of the proposed model is conceptually depicted in Fig. 1. For a given set of DC node voltages (V_{GB}, V_{DB}, V_{SB}), the evaluation of the corresponding DC drain current I_{DC} begins by calculating the transistor's modulated threshold voltage and the associated pinch-off voltage. From there, all the variables of the modified UCCM equation are set and the modulated normalized source and drain inversion charges, as well as the normalized saturation drain charge can be determined by using the 443 algorithm to solve the modified UCCM equations (6). Once the charges are computed, they are introduced in the current equation (2) to evaluate the DC drain current of the transistor.

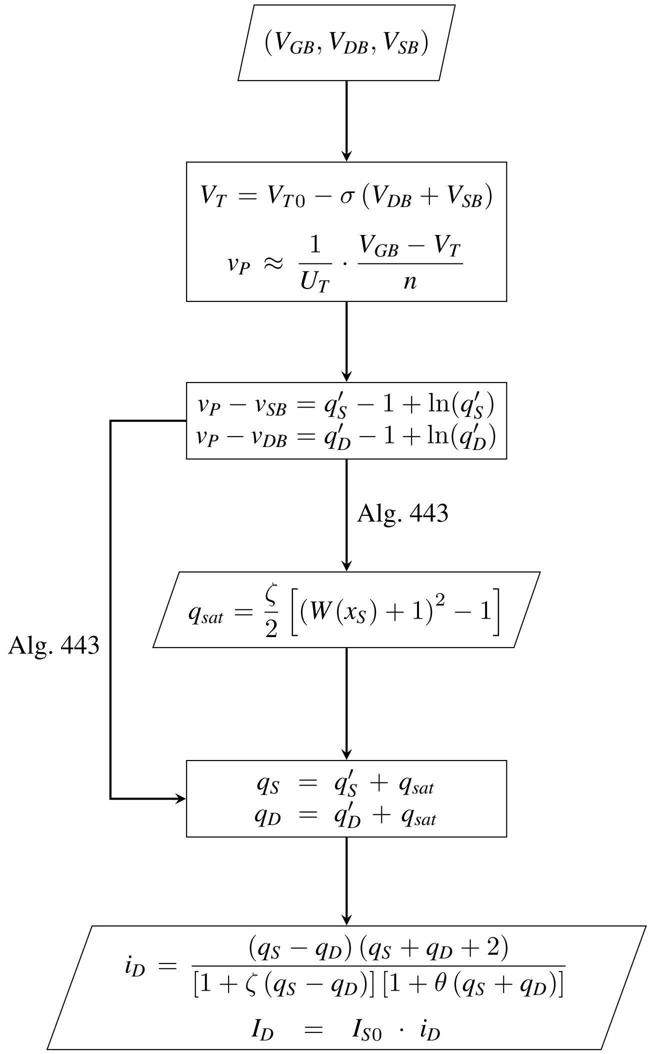

FIGURE 1: Conceptual flowchart for DC current evaluation using the proposed model and the acm 443 numerical solver.

Although the acm 443 algorithm is computationally very efficient, resorting to a numerical solver makes the model difficult to manipulate for initial hand calculations and hinders the intuitive understanding of the transistor behavior.

III. EXPLICIT $I - V$ 6PM MODEL

This section introduces a closed-form expression for the drain current I_D as a function of the transistor's node voltages, derived from the previously presented model. This explicit $I - V$ model circumvents the need for numerical solvers by utilizing an analytical approximation of the Lambert W-function. Our proposed formulation yields an explicit, single-piece equation that captures the DC drain current's dependence on node voltages with remarkable precision. The benefits of an analytical and explicit $I - V$ expression are multiple. Firstly, it facilitates an intuitive understanding of the transistor operation and the effect of short-channel effects. Moreover, the proposed formulation for the drain current is continuous and derivable, which allows us to provide explicit expressions for the transistor small signal parameters.

In the following subsections, we present the analytical approximation of the Lambert W-function and derive the proposed explicit expressions of the inversion charges, drain current and transistor small signal transconductance as a function of the transistor DC node voltages.

A. LAMBERT W-FUNCTION APPROXIMATION

Instead of relying on a numerical solver, in this paper we propose a novel formulation of the solution to the UCCM equations that allows us to get an explicit and single-piece equation linking the transistor's DC drain current and its node voltages.

Using analytical expressions instead of numerical solvers has its benefits. Firstly, it enables a faster and more efficient exploration of the design space, leading to a better understanding of the circuit performances and their relationship with the physics of the transistor. Moreover, it will be shown that the proposed formulation is derivable, and hence, it facilitates to establish links between circuit performances, usually related to the derivatives of the drain current, and the transistor parameters.

The formulation of the proposed explicit $I - V$ model is based on a recently published approximation of the Lambert W-function [21]. As seen before, the normalized source and drain charge ratios are determined by evaluating the Lambert W-function, which is the solution to the transcendental equation defined as

$$W(x)e^{W(x)} = x. \tag{17}$$

This function has two real branches. The branch of interest for our study is the one for $x \in \left[-\frac{1}{e}, \infty\right[$, which is called the principal branch and contains the domain of application of our model, defined from (13), as $x \in [0, \infty[$.

From [21], the Lambert W-function, for $x \geq 0$, can be approximated by the terms of the series,

$$W_0(x) = \ln\left[1 + \alpha(x)x\right], \tag{18}$$

$$W_n(x) = \frac{W_{n-1}(x)}{1 + W_{n-1}(x)}\left[1 + \ln\left(\frac{x}{W_{n-1}(x)}\right)\right], \tag{19}$$

where $n = 1, 2, 3\ldots$, and function $\alpha(x)$ is defined by

$$\alpha(x) = \frac{1}{1 + \dfrac{\ln(1 + x)}{2}}. \tag{20}$$

The approximation of the Lambert W-function improves as n increases. For $n = 0$, the maximum relative error in the approximation for all the considered branch is below 4%. For $n = 1$ this error is reduced below 0.022%. The series matches the accuracy of numerical solvers for $n = 3$.

In this work, we will employ the approximation $W(x) \approx W_0(x)$, which gives us a good trade-off between model complexity and accuracy.

B. EXPLICIT $q_{s(d)}$ AND I_D EXPRESSIONS AS A FUNCTION OF THE TRANSISTOR'S NODE VOLTAGES

Based on the proposed approximation of the Lambert W-function, the modulated normalized source and drain inversion charges can be obtained from equations (12), (13), and (18) as,

$$q'_{S(D)} = \ln\left[1 + \frac{e^{v_P - v_{S(D)B}+1}}{1 + \frac{1}{2}\ln\left(1 + e^{v_P - v_{S(D)B}+1}\right)}\right]. \tag{21}$$

Equation (21) can be expanded in order to get a continuous single-piece expression for the normalized source and drain inversion charges dependent on the transistor's terminal voltages, which leads to (22).

Similarly, the explicit expressions of the normalized charges (22) can be directly injected in (2) to obtain a continuous single-piece explicit equation for the transistor's DC drain current expressed as a function of the transistor's node voltages as (27), where A, B, C, and D are defined as,

$$A = W_0(x_S) - W_0(x_D), \tag{23}$$

$$B = W_0(x_S) + W_0(x_D), \tag{24}$$

$$C = W_0^2(x_S) - W_0^2(x_D), \tag{25}$$

$$D = W_0^2(x_S) + W_0^2(x_D). \tag{26}$$

The obtained I_D approximation makes no assumption on the values of the DC node voltages and hence it is valid in all regions (linear to saturation) and regimes of operation (weak to strong inversion).

C. EXPLICIT g_m EXPRESSION AS A FUNCTION OF THE TRANSISTOR'S NODE VOLTAGES

The obtained explicit $I - V$ model is continuous and derivable, which allows to compute, analytically, the small signal parameters of the transistor. Thus, the small signal transconductance g_m of the transistor can be directly evaluated as,

$$g_m = \frac{\partial I_D}{\partial V_{GS}}. \tag{28}$$

Before computing the derivative, it is convenient to rear-

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$$q_{S(D)} = \ln\left[1+\frac{e^{v_P - v_{S(D)B}+1}}{1+\frac{1}{2}\ln\left(1+e^{v_P - v_{S(D)B}+1}\right)}\right]\left[1+\frac{\zeta}{2}\ln\left[1+\frac{e^{v_P - v_{S(D)B}+1}}{1+\frac{1}{2}\ln\left(1+e^{v_P - v_{S(D)B}+1}\right)}\right]+\zeta\right]. \tag{22}$$

$$I_D = I_{S0}\frac{\left[(1+\zeta)A+\frac{\zeta}{2}C\right]\left[(1+\zeta)B+\frac{\zeta}{2}D+2\right]}{1+\zeta\left[(1+\zeta)A+\frac{\zeta}{2}C\right]+\theta\left[(1+\zeta)B+\frac{\zeta}{2}D\right]+\zeta\theta\left[(1+\zeta)A+\frac{\zeta}{2}C\right]\left[(1+\zeta)B+\frac{\zeta}{2}D\right]}. \tag{27}$$

range the DC current equation (2) as,

$$i_D = \frac{E\,(F+2)}{1+\zeta E+\theta F+\zeta\theta EF}, \tag{29}$$

where E and F are given by,

$$E = (1+\zeta)\,A + \frac{\zeta}{2}C, \tag{30}$$

$$F = (1+\zeta)\,B + \frac{\zeta}{2}D. \tag{31}$$

Simply applying the definition of the transconductance (28), we can arrive to a single-piece closed-form expression for the transistor's small signal transconductance that, again, is valid in all regions and regimes of operation. The equation of the transconductance is expressed in (32) as a function of the derivatives of E and F and considering that the bulk and source terminals are connected. The derivatives of E and F are detailed in the Appendix in equations (40) and (41).

IV. RESULTS

The accuracy of the proposed design-oriented 6PM model is demonstrated with direct comparisons to simulation and measurement results. These comparisons were conducted using NMOS transistors of different lengths in 28nm FD-SOI technology from STMicroelectronics. Firstly, to verify the accuracy of the proposed formulation, the proposed model is compared to an industrial production-level transistor model, the UTSOI2 [25] [26] included in the Process Design Kit (PDK) of the 28nm FD-SOI technology, it has to be noted that this industry-standard model is fully continuous and highly configurable. Then, the proposed 6PM model is compared to a previously published state-of-the-art design-oriented model employing 5 DC model parameters [15]. Additionally, both the numerical implementation and the explicit analytical approximation of the proposed 6PM model are considered in order to show the accuracy of the proposed explicit expressions. Finally, the proposed 6PM model is compared to actual characterization measurements on a set of fabricated transistors in the selected 28nm FD-SOI technology.

In our validation, we employ NMOS transistors with lengths of 30 nm, 60 nm, and 150 nm, in order to show the dependency of the model parameters with the transistor length. The 30 nm transistor was chosen to highlight the ability of the proposed model to accurately describe the short-channel effects, while the 150 nm transistor was chosen to represent a long-channel transistor. Moreover, due to an optical shrink during the process, a length of 30 nm represents the minimal length in STMicroelectronics 28 nm FD-SOI CMOS technology, and lengths of 60 nm and 150 nm are commonly used in analog and RF design [27] [28] [29] [30] [31] [32], making them practical choices for this study. The DC model parameters employed to build the design-oriented 6PM model were obtained using the extraction methodology described in [14], [33] for each of the considered transistor's lengths. The set of extracted model parameters for the three considered transistor's lengths are listed in Table 2.

TABLE 2: Design-oriented 6PM model parameters for 28nm FD-SOI NMOS transistors ($W = 1\,\mu m$ for all considered transistors).

L	30 nm	60 nm	150 nm
n	1.31	1.16	1.11
V_{T0} (mV)	352	388	414
I_{S0} (μA)	4.58	3.25	1.4
σ	0.093	0.023	0.0082
ζ	0.026	0.014	0.008
θ	0.039	0.041	0.018

Additionally, as previously discussed in Section II, it is also possible to derive geometrical scaling laws to explicitely take into account the dependency in L of each model parameter, as demonstrated in [24]. As an illustration, we extracted a fourth-order polynomial law for the equilibrium threshold voltage, V_{T0}, depicted in Fig. 2, to show the feasibility of this approach.

A. SIMULATION RESULTS

Simulation results were obtained for a common source configuration of the transistor, as depicted in Fig. 3, connecting the source to the bulk, i.e., $V_S = V_B = 0\,V$. Using this configuration, Fig. 4, 5, and 6 represent the obtained I_D-V_{GB} and I_D-V_{DB} curves for different values of V_{GB} for the former and V_{DB} for the latter. It is noteworthy that the common-source topology is, to our knowledge, the most widely used topology in many analog, RF, and mmW designs implemented in integrated circuits, especially in CMOS technologies.

The considered voltage sweeps cover all operation regions and regimes of the transistor. Fig. 4 corresponds to a short-channel transistor with a length of $L = 30$ nm, Fig. 5 corresponds to $L = 60$ nm and Fig. 6 corresponds to a long-

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$$g_m = \frac{I_{S0}}{U_T}\frac{\left[E'\left(F+2\right)+EF'\right]\left[1+\zeta E+\theta F+\zeta\theta EF\right]-E\left[F+2\right]\left[\zeta E'+\theta F'+\zeta\theta\left(E'F+F'E\right)\right]}{\left[1+\zeta E+\theta F+\zeta\theta EF\right]^2}. \tag{32}$$

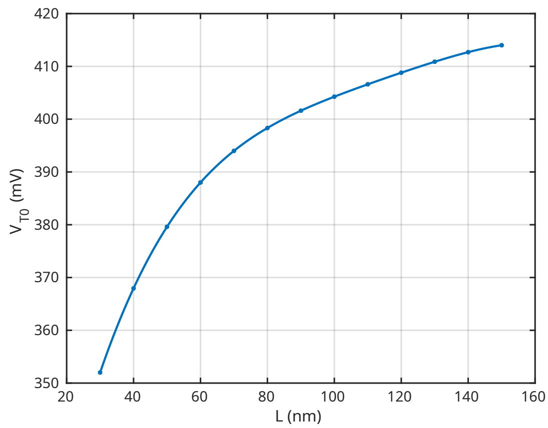

FIGURE 2: **Extracted geometrical scaling law of the equilibrium threshold voltage V_{T0} of 28 FD-SOI NMOS transistor.**

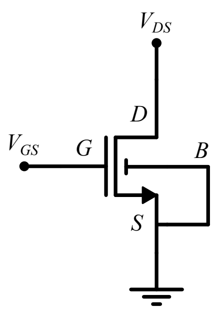

FIGURE 3: **Common source configuration.**

channel transistor of $L = 150\,\text{nm}$. All transistors have a width of $W = 1\,\mu$m. Fig. 7 shows the I_D-V_{GB} curves in semilog scale to highlight the modeling of the subthreshold region for the three considered transistor's lengths.

Additionally, to better highlight the dependency of the drain current with the geometrical dimension of the transistor, W and L, Fig. 8 illustrates a three-dimensional representation of I_D as a function of the channel width W and length L, at a constant gate-to-bulk voltage V_{GB} and drain-to-bulk voltage V_{DB} of $0.5V$, with the source-to-bulk voltage V_{SB} set to $0V$.

Fig. 4, 5, 6, and 7 offer a direct comparison between the proposed design-oriented 6PM model (both numerically computed based on 443 algorithm and analytical based on explicit expressions), the industry-standard UTSOI2 compact model, and the 5PM design-oriented model of [15] based on 443 algorithm resolution. Additionally, we represent also the relative error of the proposed 6PM model (both numerical and analytical solutions) with respect to the UTSOI2 model. For Fig. 4, 5, 6, and 7, the proposed relative errors are defined as follows:

$$Rel.Error_{An.Res} = \frac{I_{D,\,An.Res} - I_{D,\,UTSOI2}}{I_{D,\,UTSOI2}}, \tag{33}$$

$$Rel.Error_{443} = \frac{I_{D,\,An.Res} - I_{D,\,443}}{I_{D,\,443}}. \tag{34}$$

As it can be seen, the proposed design-oriented 6PM model offers a very good approximation of the transistor behavior, very close to the UTSOI2 curves. Compared to the previously presented 5PM design-oriented model, the introduction of the mobility reduction parameter, θ, not present in the 5PM model, allows us to better model the transistor behavior for strong values of V_{GS}, both for short-channel and long-channel transistors.

The proposed model is considered design-oriented due to its simplicity and its precision in characterizing the behavior of the transistors. In this regard, designers often employ specific transistor metrics –other than the drain current– to correlate their circuit specifications with the transistors' capabilities. Analog designers typically utilize the transistor's transconductance g_m, which is closely associated with analog specifications such as the gain of an amplifier. In contrast, digital designers frequently consider the I_{on}/I_{off} ratio as a significant metric to evaluate the energy efficiency of a technology, where I_{on} and I_{off} are defined as,

$$I_{on} = I_D|_{V_{GS}=V_{DS}=V_{DD}}, \tag{35}$$

$$I_{off} = I_D|_{V_{GS}=0V, V_{DS}=V_{DD}}. \tag{36}$$

Thus, Fig. 9 shows a direct comparison between the proposed explicit expression for the transistor's transconductance g_m and the transconductance evaluated from the UTSOI2 model. In order to highlight the contribution of the mobility reduction parameter θ to g_m, we have plotted the complete analytical expression (32), and the same expression neglecting the mobility reduction contribution by making $\theta = 0$. As it can be seen, the complete 6PM analytical expression follows closely the UTSOI2 model. On the other hand, neglecting the mobility reduction effect leads to an overestimation of g_m for moderate and strong values of V_{GS}.

Finally, Fig. 10 presents a comparative analysis of the I_{on}/I_{off} ratio. The ratio obtained using the proposed explicit expression for the drain current I_D is compared against the results derived from the UTSOI2 model. To better highlight the impact of mobility reduction and the advantage of our proposed 6PM model, we have illustrated the obtained I_{on}/I_{off} ratio using both the complete analytical expression of I_D as per equation (27) and the same expression with $\theta = 0$, thereby omitting the mobility reduction effect. The findings are consistent with the transconductance analysis; the comprehensive 6PM analytical expression closely mirrors the

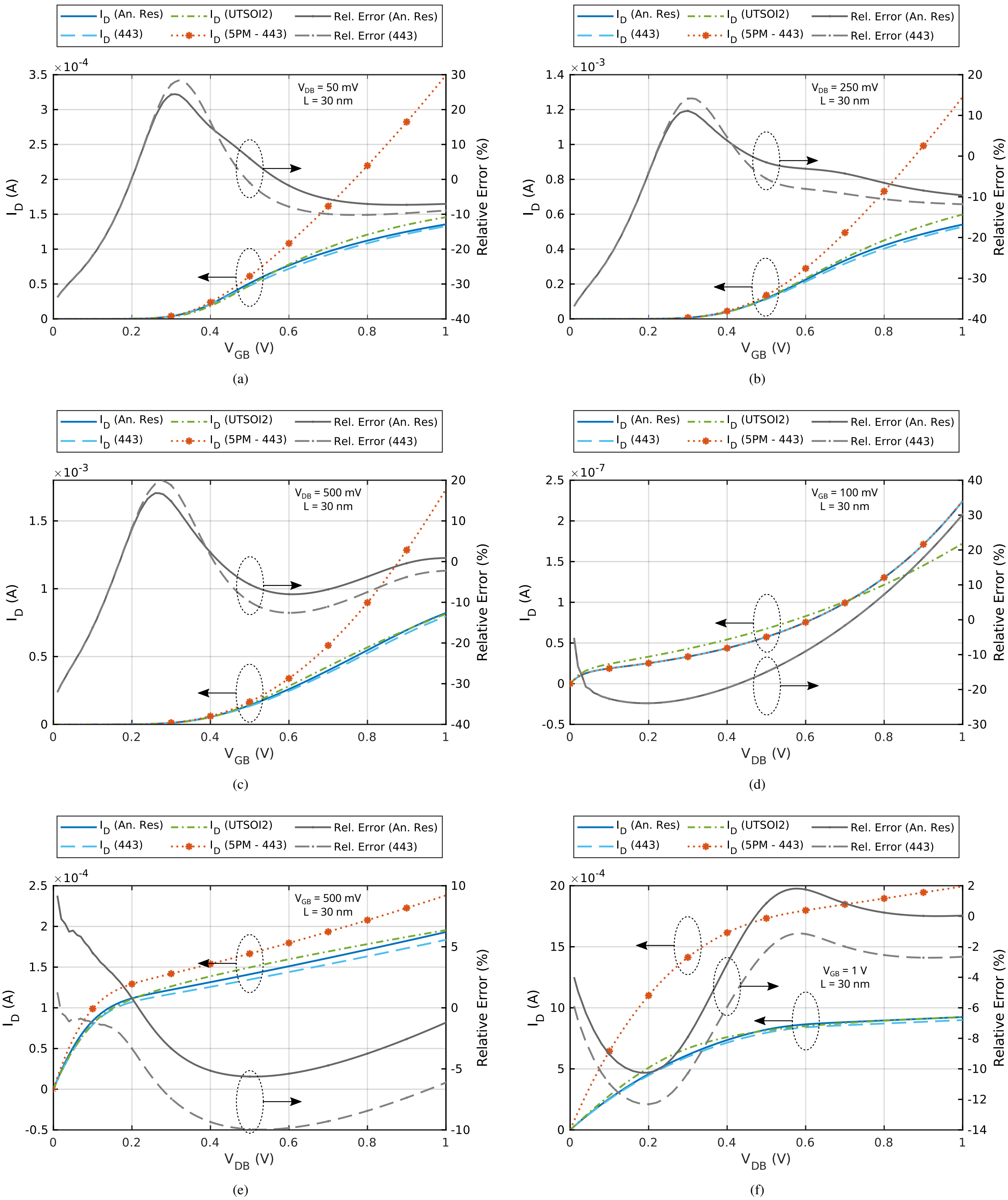

FIGURE 4: Comparison with simulation: I_D-V_{GB} (V_D = 50 mV (a), V_D = 250 mV (b), and V_D = 500 mV (c)) and I_D-V_{DB} (V_G = 100 mV (d), V_G = 500 mV (e), and V_G = 1 V (f)) curves of 28 FD-SOI NMOS transitor with L = 30 nm and W = 1 μm.

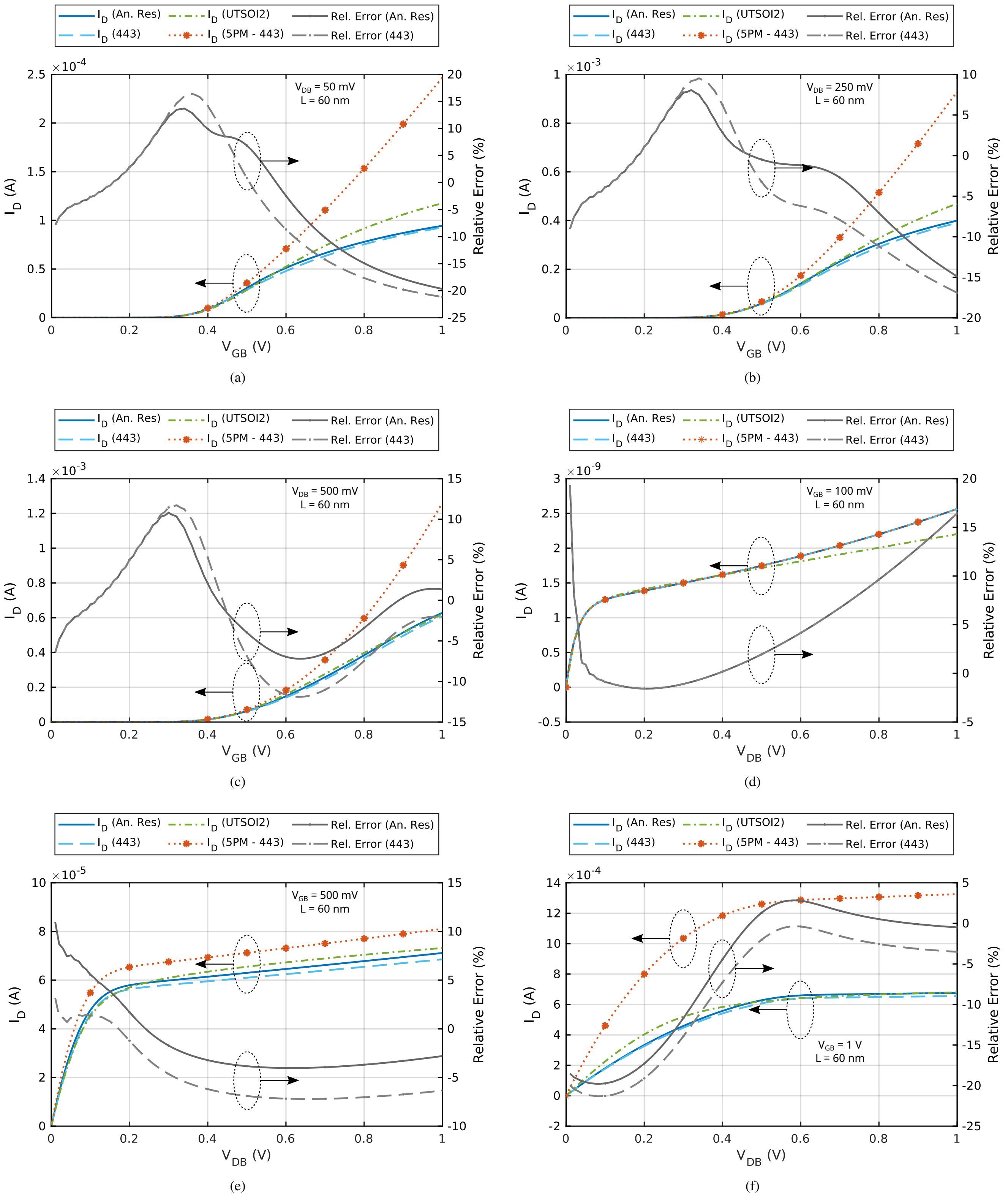

FIGURE 5: Comparison with simulation: I_D-V_{GB} (V_D = 50 mV (a), V_D = 250 mV (b), and V_D = 500 mV (c)) and I_D-V_{DB} (V_G = 100 mV (d), V_G = 500 mV (e), and V_G = 1 V (f)) curves of 28 FD-SOI NMOS transitor with L = 60 nm and W = 1 μm.

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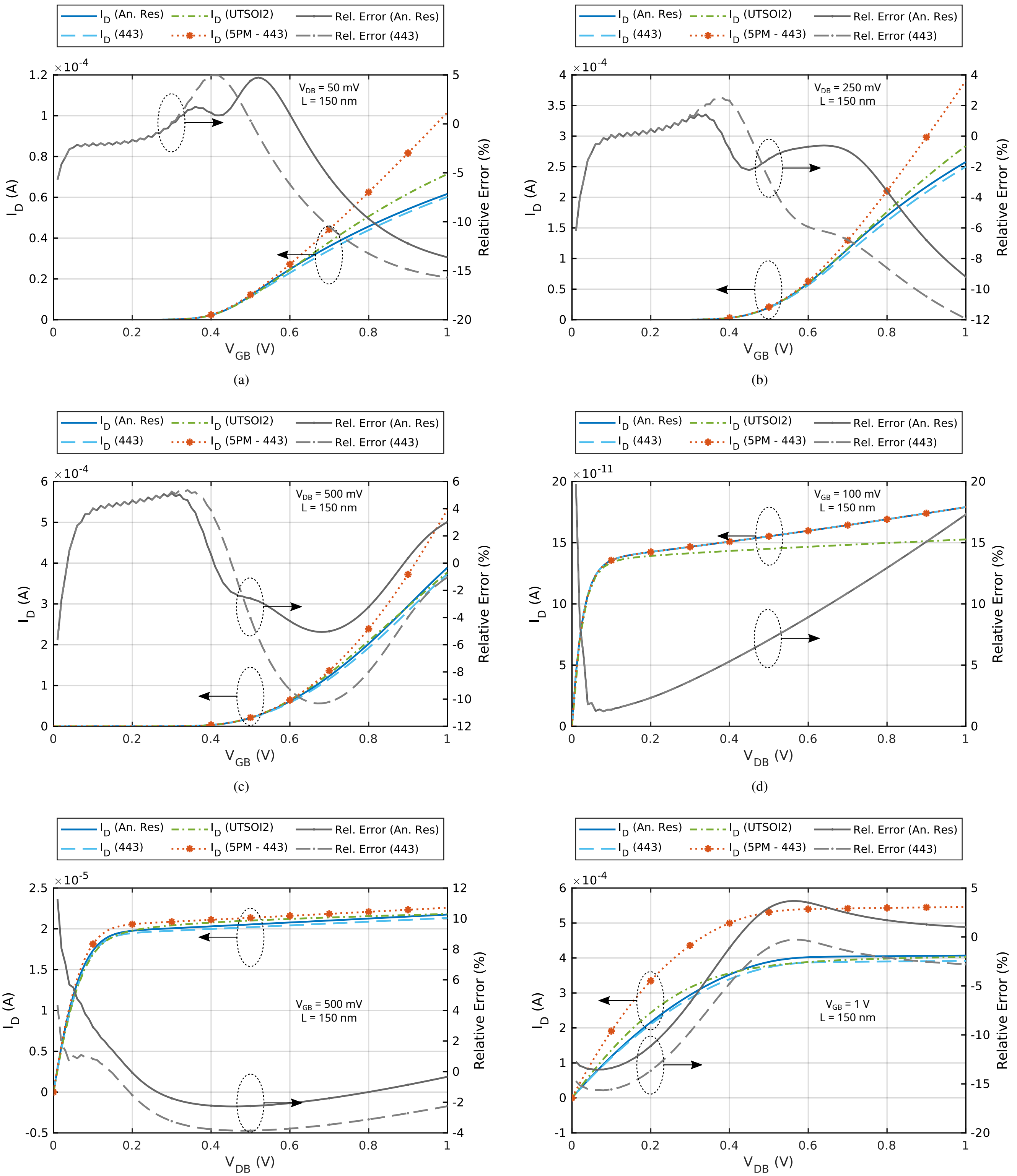
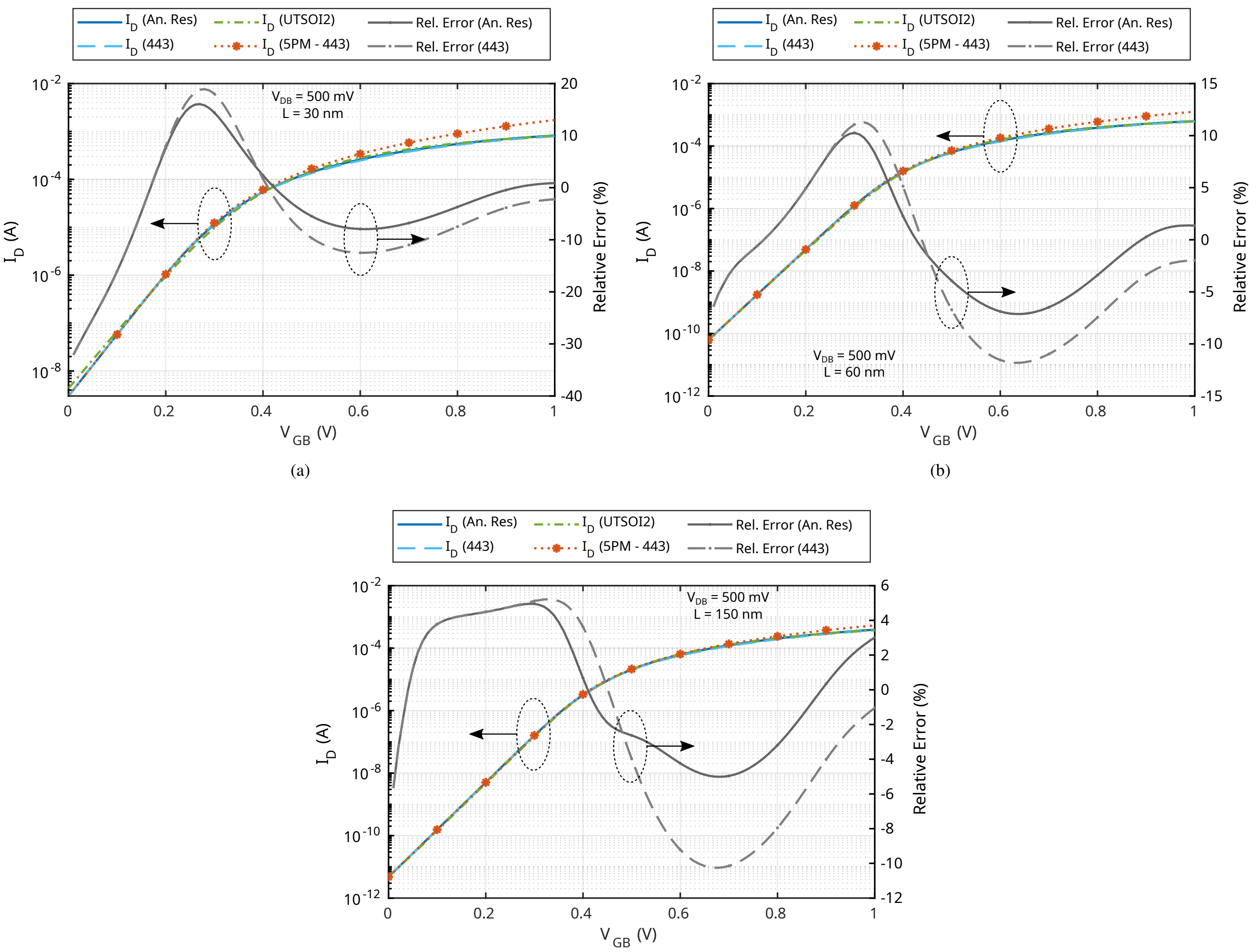


FIGURE 6: Comparison with simulation: I_D-V_{GB} (V_D = 50 mV (a), V_D = 250 mV (b), and V_D = 500 mV (c)) and I_D-V_{DB} (V_G = 100 mV (d), V_G = 500 mV (e), and V_G = 1 V (f)) curves of 28 FD-SOI NMOS transitor with L = 150 nm and W = 1 μm.



(a) (b) (c)

FIGURE 7: Comparison with simulation: I_D-V_{GB} (V_D = 500 mV) curves of 28 FD-SOI NMOS transitor with L = 30 nm (a), 60 nm (b), and 150 nm (c) and W = 1 μm in semilog scale.

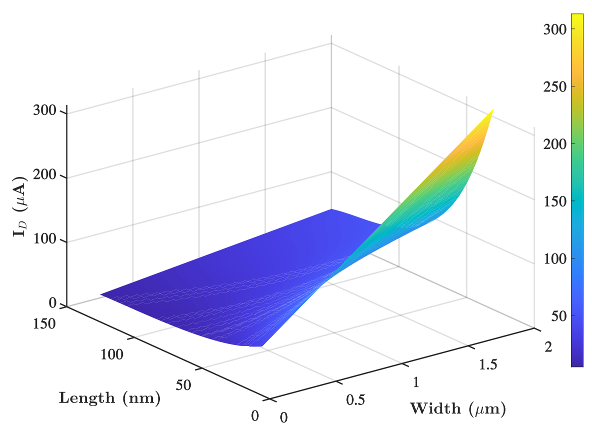


FIGURE 8: Three-dimensional plot of the drain current I_D as a function of the transistor channel width W and length L at V_{GB} = V_{DB} = 0.5V and V_{SB} = 0V, using the proposed ACM 6PM.

UTSOI2 model. Conversely, once strong inversion is established, disregarding the mobility reduction effect results in an overestimation of the I_{on}/I_{off} ratio.

In summary, Fig. 4, 5, 6, 7, 9, and 10 highlight the key contributions of the proposed model. Firstly, they demonstrate the precision of the approximation, validating the implementation of the proposed model. Secondly, they underscore the necessity of introducing the mobility reduction factor θ, to enhance accuracy across all the operating regions and regimes of the transistor. Furthermore, it is noteworthy that the introduction of the mobility reduction factor θ mathematically introduces a new pole compared to the I_D expression of the 5PM ACM model presented in [16]. This theoretical addition accounts for the differences observed between the 5PM curves and those of the model presented in this paper.

B. MEASUREMENT RESULTS

Figures 11 and 12 show a comparison between the proposed closed-form 6PM design-oriented model and experimental characterization measurements for a set of fabricated NMOS transistors in STMicroelectronics 28nm FD-SOI technology.

Fig. 11 shows the obtained I_D-V_{GB} curves for V_{DS} = 500 mV and I_D-V_{DB} curves for V_{GS} = 500 mV, for the three considered transistor's lengths, L = 30 nm, L = 60 nm and L = 150 nm. As can be seen, the proposed analytical model approximates closely the measured behavior of the transistor.

Finally, Fig. 12 shows a comparison between the analytical expression for the transistor's tranconductance g_m, and the transconductance evaluated from the transistor's characterization measurements. Again, it is clear to see that the proposed closed-form expression follows the behavior observed in the experimental measurements.

The various measurement results corroborate the conclusions drawn from the simulation results: the necessity of introducing of the mobility reduction factor θ, and the precision of the new approximation leading to the novel implementation of the proposed model. The close agreement between the measurement data and our proposed model, both qualitatively and quantitatively, reinforces the notion that the proposed model could be a highly useful tool for preliminary design. It could serve both analog and digital designers and offers a valuable asset for easily characterizing new technologies through simple DC measurements on individual transistors.

V. DISCUSSION

In the view of the obtained simulation and measurement results, we observe a compelling alignment between the behavior of our simple 6PM model and the industry-standard UTSOI2 model. Moreover, this alignment is observed for both the numerically computed model using the 443 algorithm and for the proposed analytical approximation that offers, for the first time, a single-piece explicit $I - V$ equation for the transistor DC behavior valid for all inversion regions and operation regimes.

Concerning possible future applications of the proposed model, the primary objective is not to replace the comprehensive UTSOI2 model provided in the technology PDKs, but to provide a streamlined alternative that can be especially beneficial during the initial stages of technology development and circuit design. For instance, in the context of a PDK that is still under development, our model offers a rapid and efficient means to characterize the technology, which can be particularly advantageous. Furthermore, the model's simplicity and analytical nature allow for swift exploration of the design space, which is crucial during preliminary design efforts.

When considering the implementation of short-channel effects, the ACM 6PM model introduced in this work strikes a good trade-off between simplicity and precision. While the ACM 7PM model incorporates a more complex approach to account for channel length modulation (CLM) in addition to DIBL and velocity saturation, our ACM 6PM model achieves a similar level of accuracy with less complexity. In this regard, the model dependency in V_D is controlled by the balance of two model parameters (i.e., σ and ζ, related to DIBL and velocity saturation, respectively). It has to be noted that the shorter the channel length, the stronger the short-channel effects are expected to be. The working principles of the model do not present a structural limitation on the scaling of the device. However, a decrease in precision could be anticipated if non-considered short-channel effects become significant for deeply scaled transistors.

In order to put our results into perspective, Table 3 offers a direct comparison between the proposed 6PM model and previous design-oriented MOSFET models presented in the literature. Table 3 presents a summary of the advantages and trade-offs associated with each model. By presenting a direct comparison with various ACM model versions and the UTSOI2 model, we aim to highlight the practical utility and analytical strengths of the proposed 6PM model in the broader context of transistor modeling. As it can be seen, the proposed 6PM model offers a comparatively good trade-off between model complexity and precision.

VI. CONCLUSION

In this paper, we have introduced a novel 6-parameter MOSFET DC model that accurately captures the main short-channel effects present in advanced nanometric technologies, such as carrier velocity saturation, DIBL, and mobility reduction, while maintaining a single-piece continuous form that is valid for all operation regions (linear to saturation) and regimes (weak to strong inversion). Moreover, we have proposed for the first time an explicit $I - V$ model based on an approximation of the Lambert W-function that avoids the use of numerical solvers and allow us to express the transistor's DC drain current and transconductance as a direct function of the node voltages.

The proposed model, based on only 6 DC parameters, offers a compelling trade-off between complexity and accuracy which makes it particularly suited for the initial characterization of new technologies, such as an in-development PDK, and for facilitating and speeding up early-stage design space exploration.

Concerning the limitations of the model, it has to be noted that it offers an approximation to the actual behavior of the MOS transistor. This approximation is aimed at helping designers with the preliminary sizing of a given design while keeping an intuitive link to the technology parameters. However, our model is not intended for fully replacing the complete compact models in the technology PDK which take into account a wide variety of nonidealities that are not considered in our model.

The accuracy of the proposed model has been thoroughly validated through simulations and measurements on NMOS transistors fabricated in STMicroelectronics 28 nm FD-SOI technology. Lengths of 30 nm, 60 nm, and 150 nm have been used to cover a range of channel sizes, from short-channel to long-channel transistors. These sizes were chosen due to their common usage in analog and RF design within this technology. Moreover, the results have been compared against the industrial production-level UTSOI2 model and previously

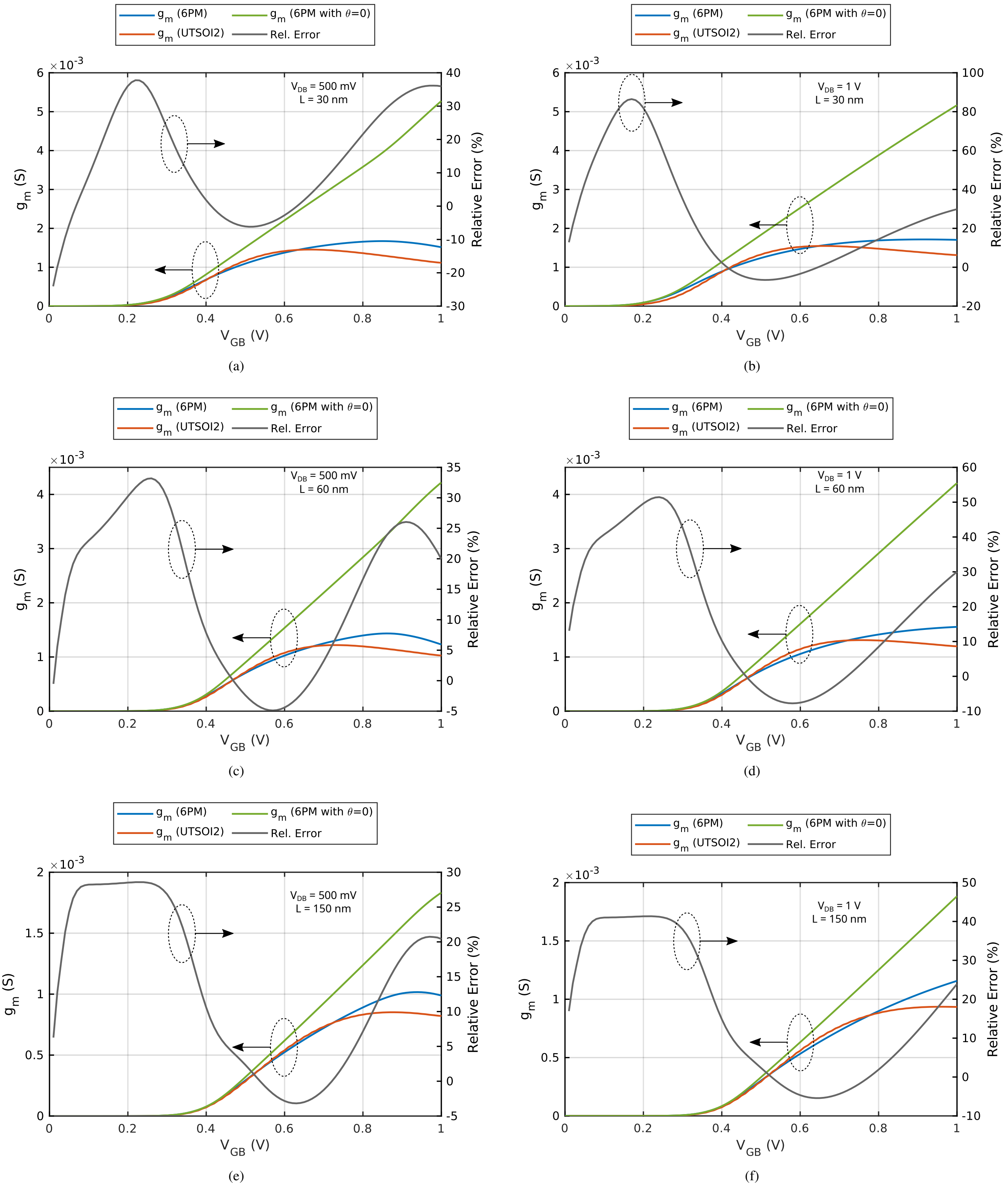


FIGURE 9: Comparison with simulation: g_m-V_{GB} for L = 30 nm (V_D = 500 mV (a), V_D = 1 V (b)), L = 60 nm (V_D = 500 mV (c), V_D = 1 V (d)), and L = 150 nm (V_D = 500 mV (e), V_D = 1 V (f)) curves of 28 FD-SOI NMOS transistor with W = 1 μm.

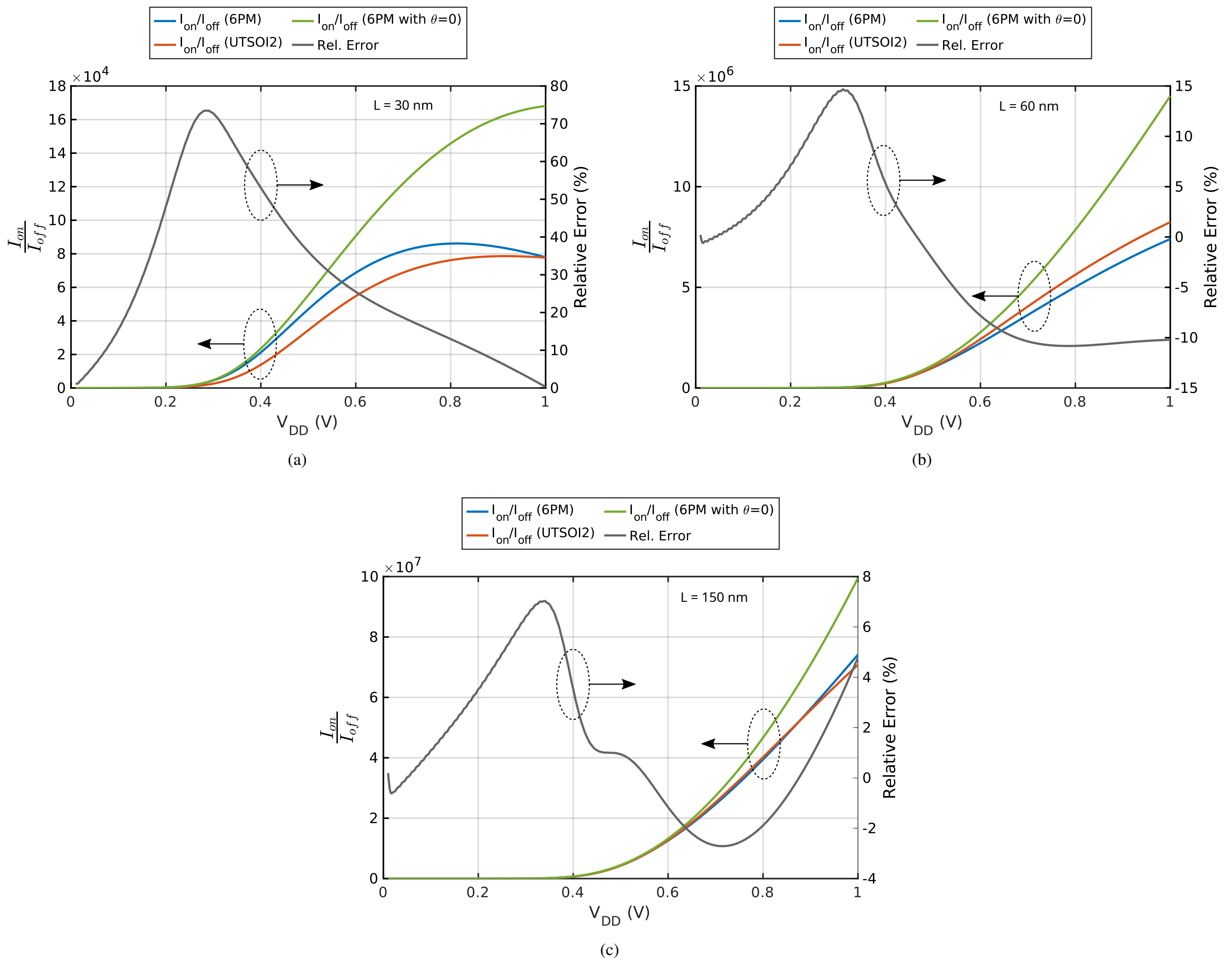


FIGURE 10: Comparison with simulation: I_{on}/I_{off}-V_{DD} for L = 30 nm (a), L = 60 nm (b), and L = 150 nm (c) curves of 28 FD-SOI NMOS transistor with W = 1 μm.

TABLE 3: Comparison between different versions of the ACM model and the industry-standard UTSOI2 model.

Features	UTSOI2 [26]	ACM 4PM [17]	ACM 7PM [14]	ACM 5PM [16]	This work
Natural transition from triode to saturation regions and weak to strong inversion zones	No	Yes	Yes	Yes	Yes
$q_i - V_{ij}$ explicit link	Not applicable	No	No	No	Yes
Number of DC parameters	tens of	4	7	5	6
Body-biasing consideration	Yes	No	No	Yes	No
I_D error [%] (*)	close to zero	32.73	4.46	12.81	5.94
Short-Channel Effects					
Velocity Saturation	Yes	No	Yes	Yes	Yes
DIBL	Yes	Yes	Yes	Yes	Yes
Mobility Reduction	Yes	No	Yes	No	Yes
CLM	Yes	No	Yes	No	No

(*) The main drain current error is calculated from $I_D - V_{GB}$ curves, in the saturation region, using the following formula: $I_{D,\,error} = \frac{1}{N}\sum_1^N |\frac{I_{D,model} - I_{D,meas}}{I_{D,meas}}|$, where N is the number of data points.

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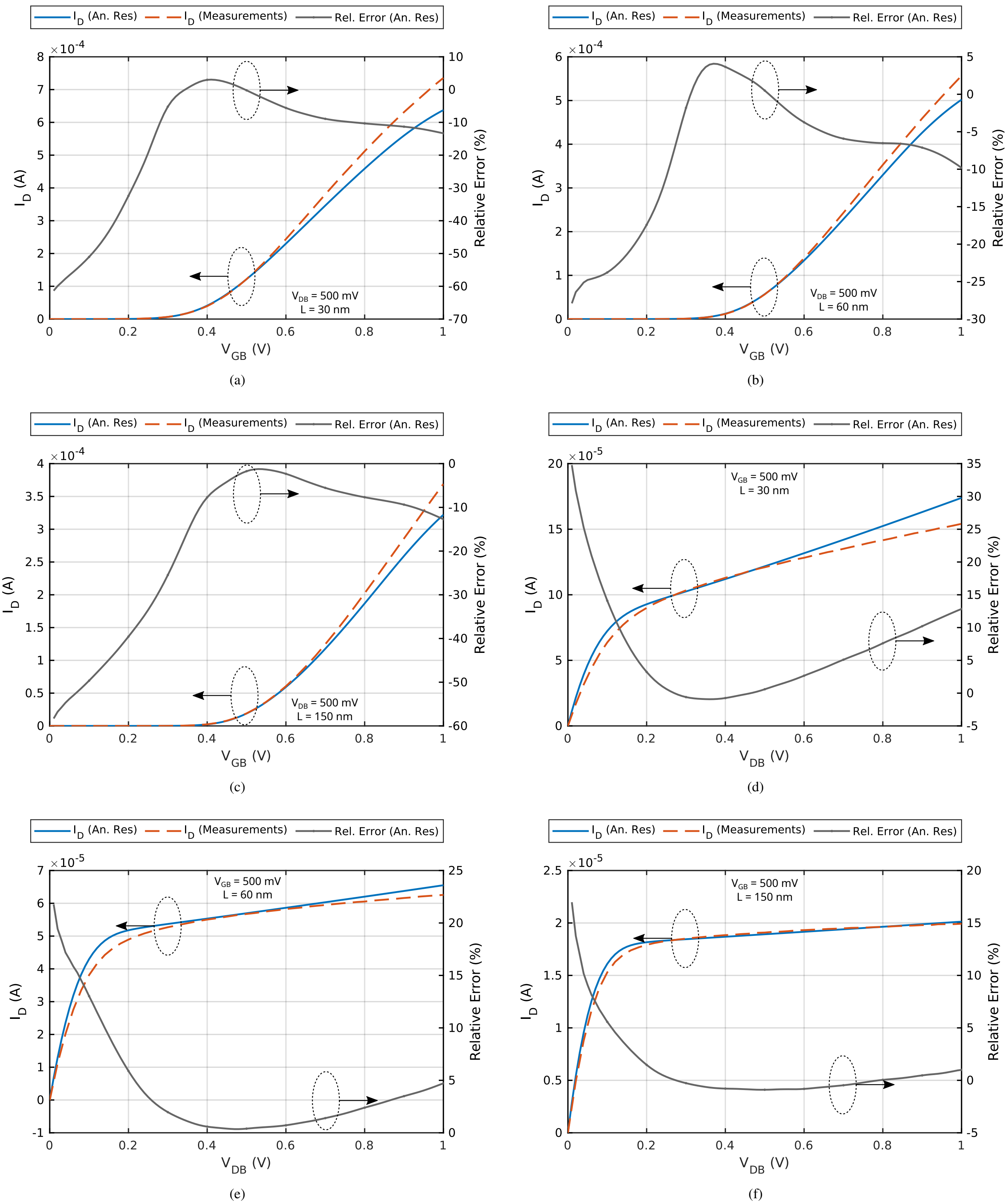

FIGURE 11: Comparison with measurements: I_D-V_{GB} at V_D = 500 mV (L = 30 nm (a), L = 60 nm (b), and L = 150 nm (c)) and I_D-V_{DB} at V_G = 500 mV (L = 30 nm (d), L = 60 nm (e), and L = 150 nm (f)) curves of 28 FD-SOI NMOS transistor with W = 1 μm.

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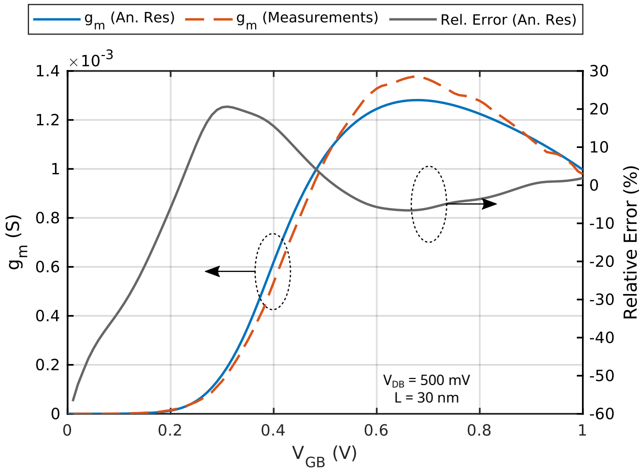
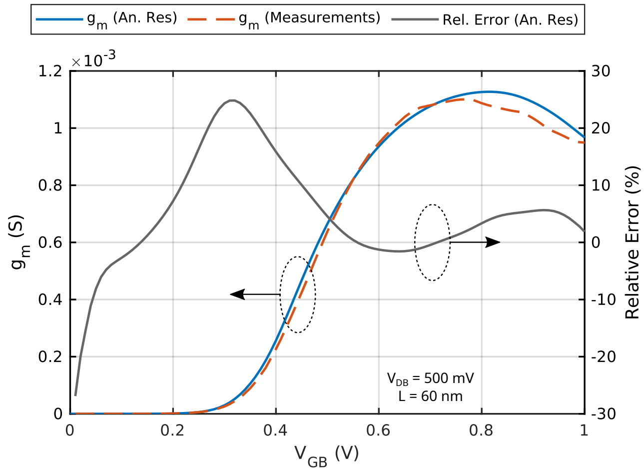
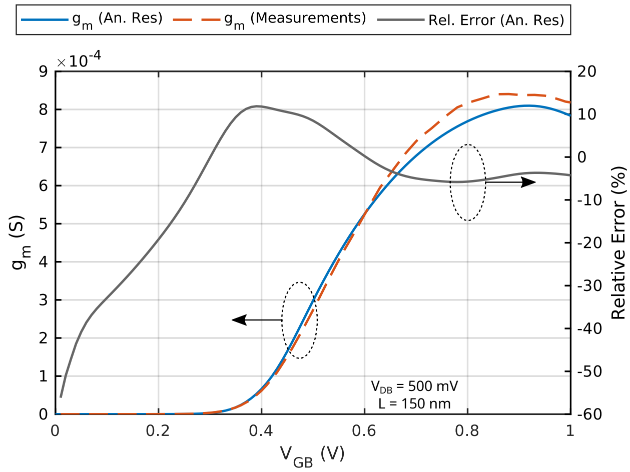


(a)



(b)



(c)

FIGURE 12: Comparison with measurements: g_m-V_{GB} for L = 30 nm (V_D = 500 mV (a)), L = 60 nm (V_D = 500 mV (b)), and L = 150 nm (V_D = 500 mV (c)) curves of 28 FD-SOI NMOS transistor with W = 1 μm.

presented state-of-the-art design-oriented MOSFET models, highlighting the accuracy and validity of the proposed model across all the considered biasing conditions.

In conclusion, the proposed 6PM model emerges as a compelling alternative to more complex models. Its accuracy, simplicity, and explicit analytical form make it an attractive option for designers seeking to navigate the complexities of modern transistor technologies. Future work can focus on extending the model to include additional non-idealities and exploring its application in various analog and digital design scenarios.

APPENDIX

A. ABBREVIATIONS AND SYMBOLS

List of abbreviations

$5PM$	5 Parameter Model
$6PM$	6 Parameter Model
ACM	Advanced Compact Model
CLM	Channel Length Modulation
$DIBL$	Drain Induced Barrier Lowering
$FD-SOI$	Fully Depleted Silicon On Insulator
IC	Inversion Coefficient
PDK	Process Design Kit
$UCCM$	Unified Charge Control Model

List of symbols

μ	Carriers effective mobility
σ	DIBL effect factor
θ	Mobility reduction factor
ζ	Carrier velocity saturation factor
C'_{ox}	Oxide capacitance per unit area
I_D	Drain current
i_D	Normalized drain current
I_{Dsat}	Normalized saturated drain current
I_{S0}	Specific current
k	Boltzmann constant
L	Channel length
L_{eff}	Effective channel length

n	Sub-threshold slope factor
q'_D	Modulated normalized inversion charge density at the drain side
q'_S	Modulated normalized inversion charge density at the source side
q	Elementary charge
Q_D	Inversion charge density at the drain side
q_D	Normalized inversion charge density at the drain side
Q_i	Inversion charge density (at the "i" side)
q_i	Normalized inversion charge density (at the "i" side)
Q_P	Pinch-off charge per unit area
Q_S	Inversion charge density at the source side
q_S	Normalized inversion charge density at the source side
q_{sat}	Normalized saturation drain charge
T	Absolute temperature
U_T	Thermal voltage
v_P	Normalized pinch-off voltage
V_{DB}	Drain to bulk voltage
v_{DB}	Normalized drain to bulk voltage
V_{GB}	Gate to bulk voltage
v_{GB}	Normalized gate to bulk voltage
V_{ij}	Voltage between terminal i and j of MOSFET (drain, source, bulk, gate)
v_{sat}	Carriers saturation velocity
V_{SB}	Source to bulk voltage
v_{SB}	Normalized source to bulk voltage
V_{T0}	Equilibrium threshold voltage
V_T	Modulated threshold voltage
W	Channel width

B. DERIVATIVES

In order to compute the derivatives of E and F let us first evaluate the derivatives of W_0 and W_0^2 as,

$$W_0'(x_{S(D)}) = \frac{\partial W_0}{\partial v_{GB}}\left(x_{S(D)}\right) = \frac{\dfrac{\Gamma_{S(D)}}{n} - \dfrac{\Gamma_{S(D)}^2}{2n\left(1+x_{S(D)}\right)}}{\Gamma_{S(D)}+1}, \quad (37)$$

and,

$$\frac{\partial W_0^2}{\partial v_{GB}}\left(x_{S(D)}\right) = 2\cdot\frac{\partial W_0}{\partial v_{GB}}\left(x_{S(D)}\right)\cdot\ln\left[\Gamma_{S(D)}+1\right], \quad (38)$$

where function $\Gamma_{S(D)}$ is given by,

$$\Gamma_{S(D)} = \frac{x_{S(D)}}{\frac{1}{2}\ln\left(1+x_{S(D)}\right)+1}. \quad (39)$$

The derivatives of E and F can be written as a function of $W_0'(x_{S(D)})$ and $\Gamma_{S(D)}$ as,

$$E' = \frac{\partial E}{\partial v_{GB}} = W_0'(x_S)\left(1+\zeta\left(1+\ln\left(1+\Gamma_S\right)\right)\right) - W_0'(x_D)\left(1+\zeta\left(1+\ln\left(1+\Gamma_D\right)\right)\right) \quad (40)$$

$$F' = \frac{\partial F}{\partial v_{GB}} = W_0'(x_S)\left(1+\zeta\left(1+\ln\left(1+\Gamma_S\right)\right)\right) + W_0'(x_D)\left(1+\zeta\left(1+\ln\left(1+\Gamma_D\right)\right)\right) \quad (41)$$

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REFERENCES

[1] J. Rabaey, *Low power design essentials*. Springer Science & Business Media, 2009.

[2] P. G. Jespers and B. Murmann, *Systematic design of analog CMOS circuits*. Cambridge University Press, 2017.

[3] F. Silveira, D. Flandre, and P. Jespers, "A g_m/I_D based methodology for the design of CMOS analog circuits and its application to the synthesis of a silicon-on-insulator micropower OTA," *IEEE Journal of Solid-State Circuits*, vol. 31, no. 9, pp. 1314–1319, 1996. DOI: 10.1109/4.535416.

[4] P. G. A. Jespers and B. Murmann, "Calculation of MOSFET distortion using the transconductance-to-current ratio (g_m/I_D)," in *2015 IEEE International Symposium on Circuits and Systems (ISCAS)*, 2015, pp. 529–532. DOI: 10.1109/ISCAS.2015.7168687.

[5] C. Enz, F. Chicco, and A. Pezzotta, "Nanoscale MOSFET modeling: Part 1: The simplified EKV model for the design of low-power analog circuits," *IEEE Solid-State Circuits Magazine*, vol. 9, no. 3, pp. 26–35, 2017. DOI: 10.1109/MSSC.2017.2712318.

[6] C. Enz, F. Chicco, and A. Pezzotta, "Nanoscale MOSFET modeling: Part 2: Using the inversion coefficient as the primary design parameter," *IEEE Solid-State Circuits Magazine*, vol. 9, no. 4, pp. 73–81, 2017. DOI: 10.1109/MSSC.2017.2745838.

[7] A. Mostafa, J. R. R. O. Martins, J. Juillard, and P. M. Ferreira, "A g_m/I_D based methodology to estimate OTA requirements in low-pass discrete time ΣΔ-ADCs," in *2024 IEEE International Symposium on Circuits and Systems (ISCAS)*, 2024, pp. 1–5. DOI: 10.1109/ISCAS58744.2024.10557892.

[8] B. Murmann, "Practical aspects of script-based analog design using precomputed lookup tables," in

2024 IEEE International Symposium on Circuits and Systems (ISCAS), 2024, pp. 1–5. DOI: 10 . 1109 / ISCAS58744.2024.10558027.

[9] J. R. R. De Oliveira Martins, A. Mostafa, J. Juillard, R. Hamani, F. De Oliveira Alves, and P. Maris Ferreira, "A temperature-aware framework on g_m/I_D-based methodology using 180 nm SOI from 40 °C to 200 °C," *IEEE Open Journal of Circuits and Systems*, vol. 2, pp. 311–322, 2021. DOI: 10 . 1109 / OJCAS . 2021.3067377.

[10] M. K. Bouchoucha, D. A. Pino-Monroy, P. Scheer, *et al.*, "Resistive feedback LNA design using a 7-parameter design-oriented model for advanced technologies," in *2023 IEEE International Symposium on Circuits and Systems (ISCAS)*, 2023, pp. 1–5. DOI: 10.1109/ISCAS46773.2023.10181341.

[11] A. Cunha, M. Schneider, and C. Galup-Montoro, "An MOS transistor model for analog circuit design," *IEEE Journal of Solid-State Circuits*, vol. 33, no. 10, pp. 1510–1519, 1998. DOI: 10.1109/4.720397.

[12] C. C. Enz, F. Krummenacher, and E. A. Vittoz, "An analytical MOS transistor model valid in all regions of operation and dedicated to low-voltage and low-current applications," *Analog integrated circuits and signal processing*, vol. 8, pp. 83–114, 1995.

[13] M. Siniscalchi, N. Gammarano, S. Bourdel, C. Galup-Montoro, and F. Silveira, "Modeling a nanometer FD-SOI transistor with a basic all-region MOSFET model," in *2020 IEEE Latin America Electron Devices Conference (LAEDC)*, 2020, pp. 1–4. DOI: 10.1109/LAEDC49063.2020.9073239.

[14] D. A. Pino-Monroy, P. Scheer, M. K. Bouchoucha, *et al.*, "Design-oriented all-regime all-region 7-parameter short-channel MOSFET model based on inversion charge," *IEEE Access*, vol. 10, pp. 86 270–86 285, 2022. DOI: 10.1109/ACCESS.2022.3198644.

[15] D. G. A. Neto, C. M. Adornes, G. Maranhão, *et al.*, "A 5-DC-parameter MOSFET model for circuit simulation in QucsStudio and Spectre," in *2023 21st IEEE Interregional NEWCAS Conference (NEWCAS)*, 2023, pp. 1–5. DOI: 10 . 1109 / NEWCAS57931 . 2023 . 10198173.

[16] D. Germano Alves Neto, M. K. Bouchoucha, G. Maranhão, *et al.*, "Design-oriented single-piece 5-DC-parameter MOSFET model," *IEEE Access*, vol. 12, pp. 87 420–87 437, 2024. DOI: 10 . 1109 / ACCESS . 2024.3417316.

[17] C. M. Adornes, D. G. Alves Neto, M. C. Schneider, and C. Galup-Montoro, "Bridging the gap between design and simulation of low voltage CMOS circuits," in *2021 IEEE Nordic Circuits and Systems Conference (NorCAS)*, 2021, pp. 1–5. DOI: 10.1109/NorCAS53631. 2021.9599867.

[18] D. G. A. Neto, G. Maranhão, M. C. Schneider, and C. Galup-Montoro, "A design-oriented single-piece short-channel MOSFET model," in *2024 IEEE International Symposium on Circuits and Systems (ISCAS)*, 2024, pp. 1–5. DOI: 10 . 1109 / ISCAS58744 . 2024 . 10558311.

[19] C. Enz, H.-C. Han, C. Delignac, and T. Taris, "A comprehensive output conductance model valid in all regions of inversion," in *2024 IEEE International Symposium on Circuits and Systems (ISCAS)*, 2024, pp. 1–5. DOI: 10.1109/ISCAS58744.2024.10558500.

[20] N. Fasarakis, A. Tsormpatzoglou, D. H. Tassis, *et al.*, "Compact model of drain current in short-channel triple-gate FinFETs," *IEEE Transactions on Electron Devices*, vol. 59, no. 7, pp. 1891–1898, 2012. DOI: 10.1109/TED.2012.2195318.

[21] R. Iacono and J. Boyd, "New approximations to the principal real-valued branch of the Lambert W-function," *Advances in Computational Mathematics*, vol. 43, Dec. 2017. DOI: 10.1007/s10444-017-9530-3.

[22] F. N. Fritsch, R. E. Shafer, and W. P. Crowley, "Algorithm 443: Solution of the transcendental equation $we^w = x$," *Communications of the ACM*, vol. 16, pp. 123–124, 1973.

[23] C. Galup-Montoro *et al.*, *MOSFET modeling for circuit analysis and design*. World scientific, 2007.

[24] J. Poupon, M. J. Barragan, A. Cathelin, and S. Bourdel, "Dynamic analysis of RF CMOS inverter-based ring oscillators using an all-region MOSFET charge-based model in 28nm FD-SOI CMOS," in *2024 IEEE International Symposium on Circuits and Systems (ISCAS)*, 2024, pp. 1–5. DOI: 10 . 1109 / ISCAS58744 . 2024 . 10558153.

[25] T. Poiroux, O. Rozeau, P. Scheer, *et al.*, "Leti-UTSOI2.1: A compact model for UTBB-FDSOI technologies — Part I: Interface potentials analytical model," *IEEE Transactions on Electron Devices*, vol. 62, no. 9, pp. 2751–2759, 2015. DOI: 10.1109/TED.2015.2458339.

[26] T. Poiroux, O. Rozeau, P. Scheer, *et al.*, "Leti-UTSOI2.1: A compact model for UTBB-FDSOI technologies — Part II: DC and AC model description," *IEEE Transactions on Electron Devices*, vol. 62, no. 9, pp. 2760–2768, 2015. DOI: 10 . 1109 / TED . 2015 . 2458336.

[27] C. Nocera, G. Papotto, A. Cavarra, E. Ragonese, and G. Palmisano, "A 13.5-dBm 1-V power amplifier for W-band automotive radar applications in 28-nm FD-SOI CMOS technology," *IEEE Transactions on Microwave Theory and Techniques*, vol. 69, no. 3, pp. 1654–1660, 2021. DOI: 10.1109/TMTT.2020.3048934.

[28] S. Sadlo, M. De Matos, A. Cathelin, and N. Deltimple, "One stage gain boosted power driver at 184 GHz in 28 nm FD-SOI CMOS," in *2021 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, 2021, pp. 119–122. DOI: 10.1109/RFIC51843.2021.9490441.

[29] G. Diverrez, E. Kerherve, M. De Matos, and A. Cathelin, "A 22-44 GHz 28nm FD-SOI CMOS 5G Doherty

power amplifier with wideband PAE_{6dBPBO} enhancement and 3:1 VSWR resiliency," in *2024 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, 2024, pp. 131–134. DOI: 10.1109/RFIC61187.2024.10600014.

[30] S. Ek, T. Påhlsson, C. Elgaard, *et al.*, "A 28-nm FD-SOI 115-fs jitter PLL-based LO system for 24–30-GHz sliding-IF 5G transceivers," *IEEE Journal of Solid-State Circuits*, vol. 53, no. 7, pp. 1988–2000, 2018. DOI: 10.1109/JSSC.2018.2820149.

[31] M. K. Bouchoucha, M. J. Barragan, A. Cathelin, and S. Bourdel, "A wideband sub-6GHz continuously tunable g_m-boosted CG low noise amplifier in 28 nm FD-SOI CMOS technology," in *ESSCIRC 2023- IEEE 49th European Solid State Circuits Conference (ESSCIRC)*, 2023, pp. 381–384. DOI: 10.1109/ESSCIRC59616.2023.10268734.

[32] T. Souvignet, B. Allard, and S. Trochut, "A fully integrated switched-capacitor regulator with frequency modulation control in 28-nm FDSOI," *IEEE Transactions on Power Electronics*, vol. 31, no. 7, pp. 4984–4994, 2016. DOI: 10.1109/TPEL.2015.2478850.

[33] R. Coitinho, L. Spiller, M. Schneider, and C. Galup-Montoro, "A simplified methodology for the extraction of the ACM MOST model parameters," in *Symposium on Integrated Circuits and Systems Design*, 2001, pp. 136–141. DOI: 10.1109/SBCCI.2001.953016.

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