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The mass production of µLEDs requires an upscaling approach on 200 mm wafers, which implies the deployment of a technology that achieves zero defectivity without liftoff. In this report, Nanoimprint lithography (NIL) processing has been successfully optimized for nanostructuring GaN-based Silicon-On-Insulator (SOI) substrates. The etching of SiO_2/GaN/AlN/Si/SiO_2 layers using different plasmas is conducted and multi-layer nanopillars 100-200 mm in diameter have been fabricated. This approach generates zero-defect arrays of pillars, which is particularly advantageous for the growth process. In addition, the SiO_2 at the bottom of the pillar allows it to twist during the subsequent GaN regrowth, as this layer becomes soft at the growth temperature >1000°C. This ability to deform enables a coalescence of pillars into layers with reduced dislocation density. As a result, high quality GaN microplatelets and µLEDs were grown via a bottom-up approach based on pendeoepitaxy using metal organic vapor phase epitaxy (MOVPE). The fabricated µLEDs have a very smooth surface with a roughness of 0.6 nm which facilitated the implementation of an easy and simple transfer protocol. Adhesive tape and metal-metal bonding, were used to bond the µLEDs onto a metal-coated silicon substrate. The reported findings in this study are highly encouraging and offer exciting new insights into the development of the next generation of high-performance displays.

1. Introduction

Over the last twenty years, displays have seen a profound evolution and have faced a number of technological issues, including the efficient and independent addressability of individual pixels, the reduction in emitting-region thickness, the increase of display size as well as improving image quality. Today, the issue of energy consumption could lead to the emergence of a new LED-based display technology. Also, the market for microdisplays is in full expansion, with the arrival of new applications that are disrupting the market. In particular, highly luminous microdisplays are required for augmented reality and projection systems. The use of μLEDs should enable the creation of better resolved, compact, low-power, high-luminous microdisplays. Consequently, this technology has been the focus of major research efforts in recent years, with the aim of developing innovative materials to meet these technological challenges.[1-4]

In this context, gallium nitride (GaN) is being extensively used for the development of micro-light emitting diodes (LEDs). However, the optoelectronic behavior and durability of these devices is highly dependent on the point defects incorporated into the active region and on the dislocation density within the GaN heterostructure. These dislocations behave as non-radiative centers, limiting the emitting capacity of such fabricated μLED. Moreover, GaN bulk substrates are very expensive compared with other semiconductors, they are only available in small diameters, and their physical and optoelectronic characteristics are still significantly far from the standards required for successful μLED processing. [5-9]

Cost-effective approaches based on GaN thin-film epitaxy on cheaper substrates, such as Si and sapphire, have been developed to circumvent the above-mentioned challenges. [10,11] Nevertheless, the epitaxy of GaN on foreign substrates still suffers from several limitations and has not completely eliminated the problems associated with dislocation density due to the large lattice mismatch. In addition, the growth of GaN on Si can lead to the appearance of cracks due to mismatch of thermal expansion coefficients between GaN and Si. One possible solution to prevent the first problem is to reduce the number of epitaxial growth sites in order to reduce the number of dislocations originating from the substrate/nuclei interface. [12,13]

Numerous approaches addressing this idea have been developed, such as growth of nanowires, selective and/or anisotropic growth of GaN on patterned substrates with and/or without dielectric masks, e.g. pendeoepitaxy (PE). [14,15] However, these strategies have been limited by

the inhomogeneous dislocation density distribution in the GaN that will be used as the active layer for the μLED. This inhomogeneity is due to the misalignment of the crystallites associated to the heteroepitaxial growth before their coalescence. [16-21]

For device fabrication, existing optical and/or electronic lithography and plasma etching techniques are able to fabricate surfaces with arrays of μLEDs. However, cathodoluminescence studies have revealed that top down etching of μLEDs creates non-emissive regions at the edges of each fabricated μLED, which greatly reduces the total optical performance of such device. In addition, this process is not suited to obtain freestanding μLEDs, that can be easily transferred to solid or flexible substrates without using highly sophisticated transfer methods.[22]

In order to overcome these physical and technological limitations, the growth of GaN crystallites on top of deformable nanopillars could be a promising, powerful and highly innovative solution. This solution has been explored in the last years and a nanoimprint lithography based patterning capability has been established.[23] However, this approach requires a lift-off step that is incompatible with 200 mm silicon production lines.

To overcome these limitations, we introduce in the present paper a new approach that does not employ liftoff at any stage, which renders it compatible with 200mm Si production lines. With the newly fabricated nanopillars via nanoimprint lithography and plasma etching, we will implement pendeopepitaxy of high-quality GaN plateletes on SOI substrates, as discussed in references, [23-25] and thereafter the growth of complete InGaN/GaN μLEDs. The size of the platelets has been defined so that each one constitutes an individual μLED. These μLEDs will be finally transferred in parallel to a carrier substrate, highlighting the scalability of the whole fabrication/growth/transfer process.

2. Results and Discussion

2.1 Fabrication of GaN-based nanopillars

The fabrication of nanopillars using the NIL and plasma etching approach with no-liftoff is a highly successful path for achieving very homogenous etching. Figure 1 illustrates in detail the seven main technological steps of this approach involved in the fabrication of GaN nanopillars. The first phase consisted in fabricating a FDTS coated Si master with the targeted pillar dimensions, i.e. 71 nm in height and 200 nm or 100 nm in diameter distributed within arrays that each measures 40x30 μm^2, as illustrated in Figure 1(1) and repeated across the 36x36 mm^2 surface. An optical image of the entire mask and an SEM zoomed view showing the hexagonal

distribution of pillars are shown in Figure 2 (a). Subsequently, as shown in Figure 1(2-3), a PDMS/HPDMS composite is deposited on the Si master in order to reproduce the inversed patterns in a flexible mold after the demolding process with a picture of the mold shown in Figure 2-b. We have selected a height of 71 nm in order to imprint the mr6000, measuring 100 nm in thickness, and maintain a residual thickness after the imprint process. The fabrication of the nanopillars from the multilayered GaN on SOI structure requires the deposition of two hard SiO_2 and Cr etching masks, with a Plassys electron beam evaporator, as displayed in Figure 1 (4). The second phase of the process focuses on the nanopatterning via nanoimprint lithography (NIL), which is considered a highly efficient and high-resolution nanotransfer patterning technique [24]. The mr6000, a temperature and UV sensitive resist, is applied to the SiO_2 hardmask surface. Then, an annealing at 95 ºC for 3 min takes place, before pressing the PDMS mold onto the annealed resist and carrying out the NIL at a pressure of 1 bar and a temperature of 75 ºC in order to crosslink the polymer and successfully transfer the pillar patterns to the polymer (figure 1 (5)). After the NIL and the demolding, we obtain a nanopatterned surface with a residual thickness of the remaining polymer (Figure 1-(6)). The dry etching of the pillars is ensured by combining several plasmas in an ICP DPS reactor (Figure 1(6-7)), and real-time monitoring of the etching process thanks to optical interferometry and measurement of the plasma emission. The monitoring process consists in illuminating the wafer under etching with a xenon lamp at wavelengths ranging from 200 to 800 nm. During etching, curves and bands corresponding to detection wavelengths (415 nm, 425 nm) can be observed. The shape and intensity of each etch-tracking signal depends strongly on the nature of the material under etching.

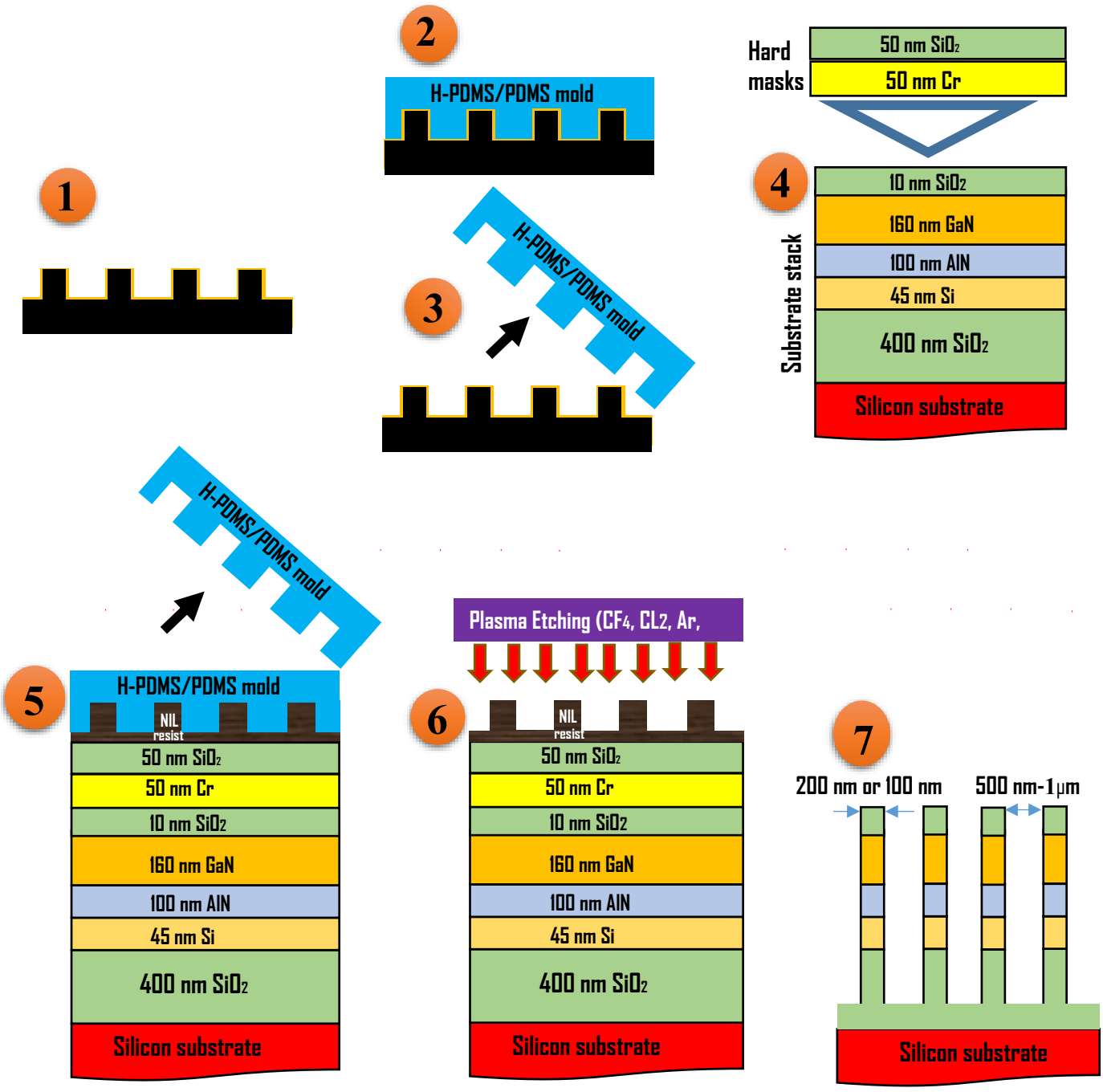

Figure 1. Fabrication pillars technology: (1) Si master with the FDTS antiadhesive layer, (2) Formation of the H-PDMS/PDMS mold, (3) demolding, (4) deposition of hard masks on the substrate stack, (5) nanopatterning of the resist surface (6) plasma etching of the structure, (7) etched GaN-based nanopillars.

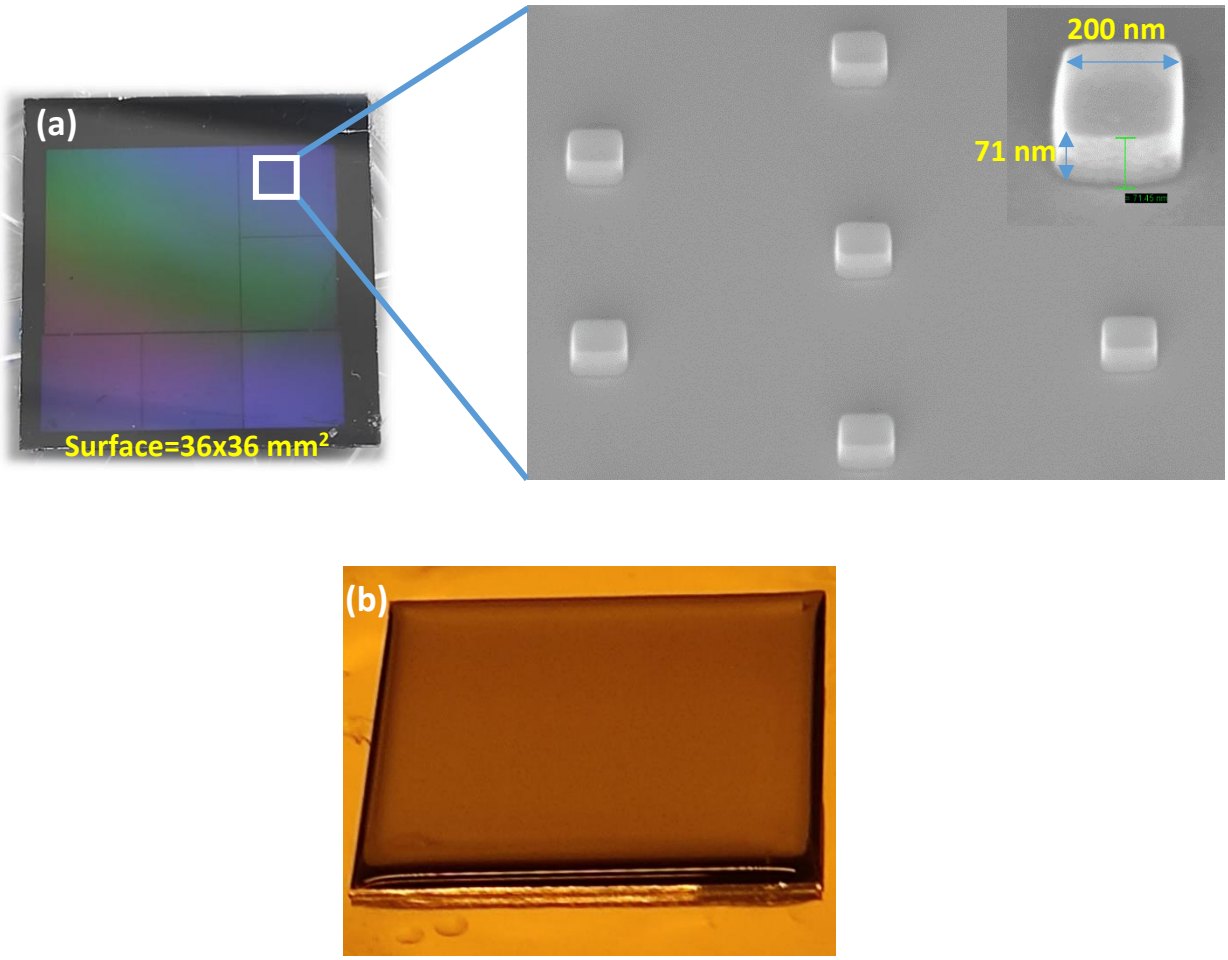

Figure 2. Fabrication of the PDMS mold: (a) image of the Si master and zoomed view of the Si pillars, (b) picture of formed HPDMS-PDMS mold on Si master.

Figure 3 shows the post-NIL pillars and related images of etching steps for the mr6000 residual thickness (rt) and hard masks (SiO_2, Cr). Controlling this rt after the NIL is an extremely critical step in our approach in order to avoid any definition problems of the nanopillars. The real-time monitoring will be exploited to track the etching in every layer except that of the rt. However, etch monitoring in real time by optical emission is very challenging. Therefore, the total etching time of this rt is carefully optimized and adjusted via several trials. The resulting texture, demonstrating the formation of PDMS pillars on the surface after NIL, is highlighted in Figure 3-a-b. The remaining resist was then etched with a plasma consisting of O_2 (30 sccm), Cl_2 (40 sccm), and Ar (80 sccm) for 40 s until reaching the SiO_2 surface as observed in Figure 3-c. Removing any residual traces of mr6000 from the surface is a critical point for avoiding any subsequent inhomogeneity in the etching process. The first SiO_2 etch mask was etched using a

CF_4-based plasma (100 sccm). As shown in Figure 3-d, the etching produced a convex profile of the top SiO_2 for the initial pillar formation.

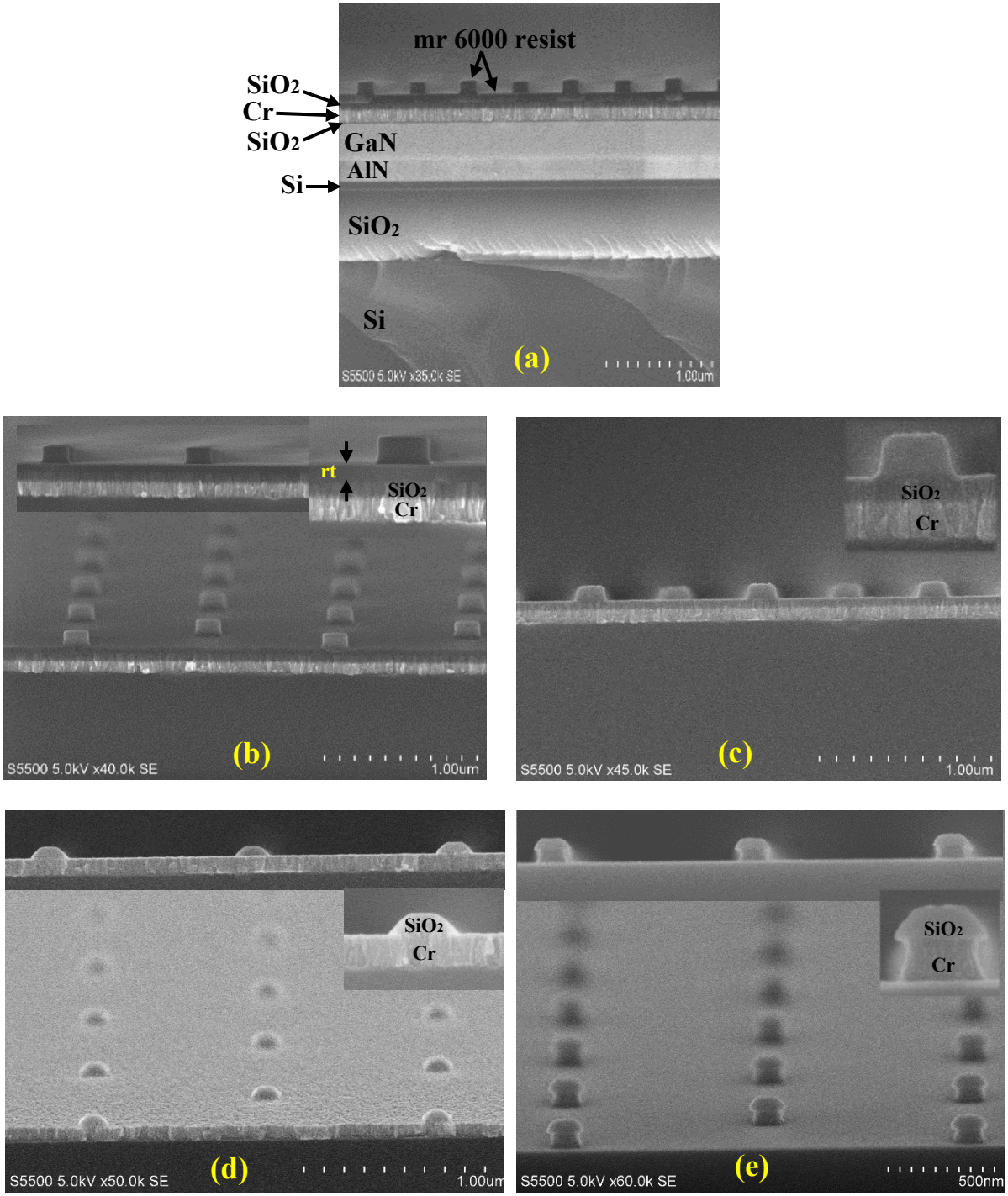

Figure 3. Etching steps of the mr6000 residual thickness (rt) and hard masks (SiO_2, Cr): (a) typical image of the entire substrate stack with the formed mr6000 pillars on the top after NIL, (b) zoomed view on the rt of the mr6000, (c) after etching of the rt, (d) SiO_2 and (e) Cr.

Next, a plasma based on Cl_2 (100 sccm) and O_2 (40 sccm) was employed to etch the Cr etch mask down to the SiO_2 surface deposited on GaN. This SiO_2 layer will be used for the masked

pendeoeptaxy in order to block the threading dislocations from the pillars and prevent their propagation in the GaN platelet, which will be used as templates for the subsequent growth of µLEDs.[25] Figure 3-d shows that the etching process forms a Cr-based profile that will be transferred to the GaN/AlN/Si/SiO_2 substrate stack for fabricating GaN-based nanopillars. This profile ensures the control of the pillar diameters and avoids the widening previously observed due to inclined etching sidewalls.[24]

The real-time tracking of each etching sequence during nanopillars development is illustrated in Figure 4. After the three etching steps described in the previous section, we start the etching of the GaN structure with a first etching of the 10 nm SiO_2 by CF_4-based plasma (step 4). Between each etched layer, we allow 15 s for stabilizing the gas flow. GaN and AlN layers were etched by Cl_2-based plasma with a gas flow of 80 sccm. As shown in the tracking spectrum, the transition from GaN to AlN is illustrated by the change in oscillation frequency (steps 5 and 6), that corresponds to a change in the etching rate. The Si and 300 nm SiO_2 are etched by CF_4 plasma (steps 7 and 8).

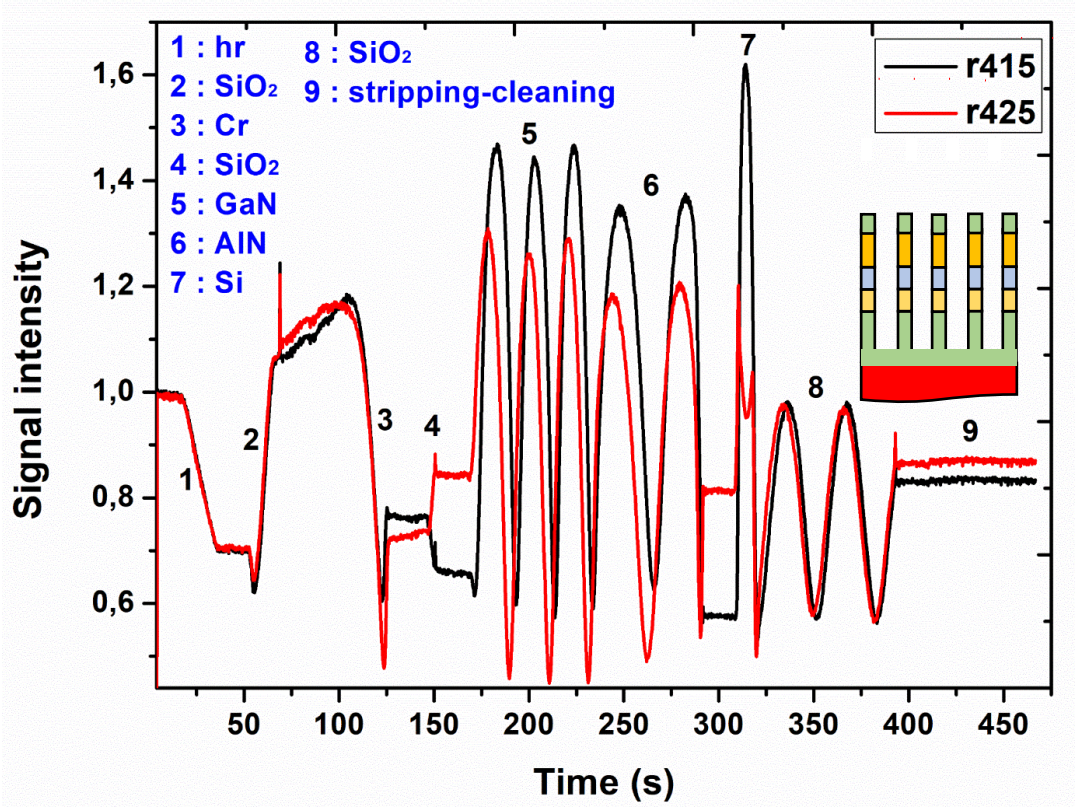

Figure 4. Real-time spectrum monitoring of rt/SiO_2/Cr/SiO_2/GaN-AlN/Si/SiO_2 layers etching for fabricating GaN-based nanopillars.

The control of this etching depth is very critical for the GaN pendeepitaxy step. Finally, the etching protocol is terminated by cleaning and stripping using O_2 plasma for 3 min in order to remove any residues from the surface.

Figure 5 shows a surface area containing several nanopillar arrays. Each array measures 30x40 μm^2 and contains pillars measuring 200 nm in diameter. The array is clearly complete, with no missing pillars. This point will be addressed in more detail in the coming section.

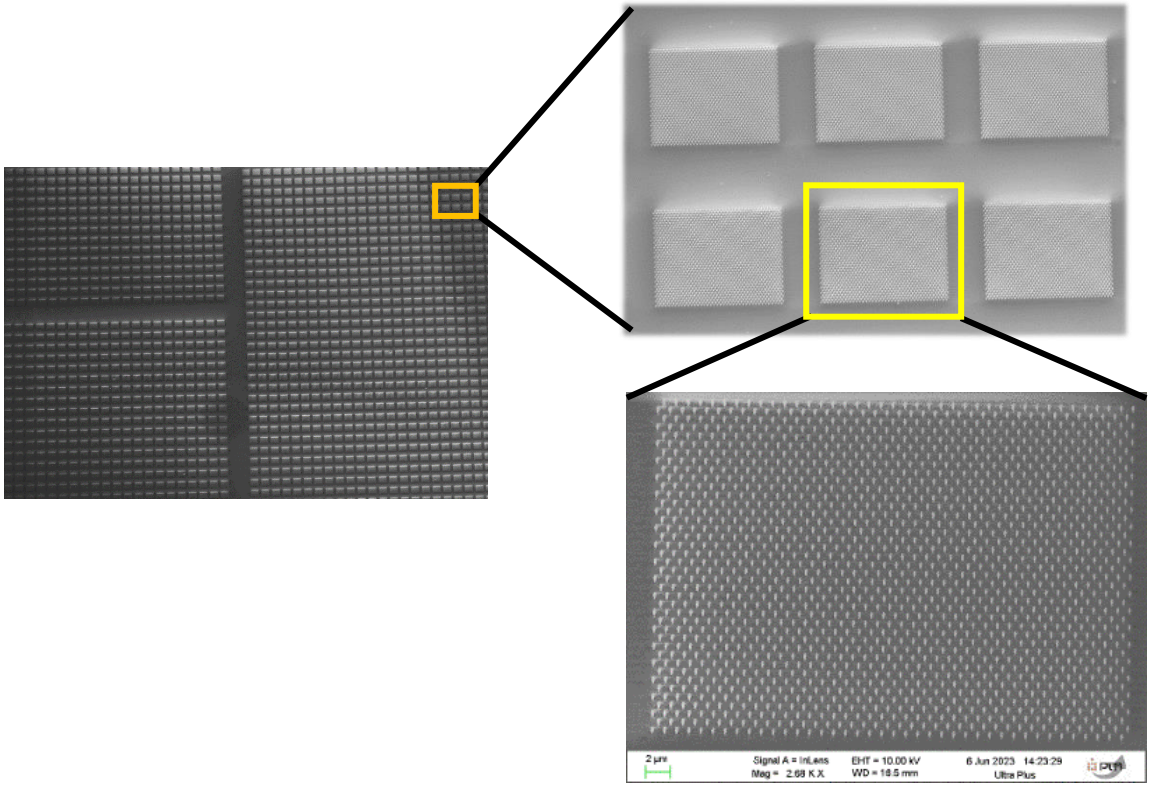

Figure 5. Etched nanopillar arrays with no missing or mis-aligned pillar.

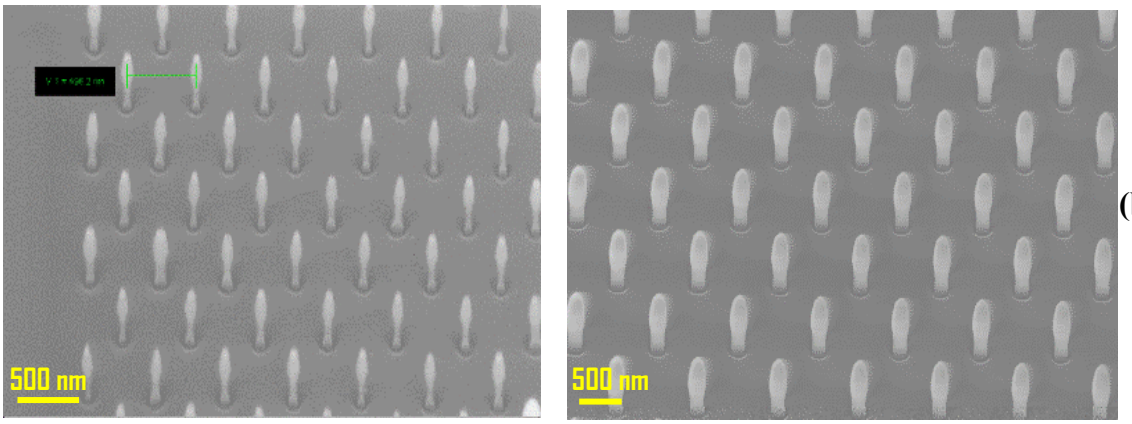

Figure 6. GaN-based nanopillars: (a) 100 nm width pillars, (b) 200 nm width pillars.

In the present report, we have used two Si masters with pillars measuring 200 and 100 nm. Figure 6 illustrates the resulting nanopillars for the two samples after etching. Nano-pillars measuring 100 nm in diameter at the top are shown in Figure 6-a. Thanks to the undercut observed during the Cr etching (Figure 3-e), the pillar diameter is 50 nm at the bottom SiO_2.

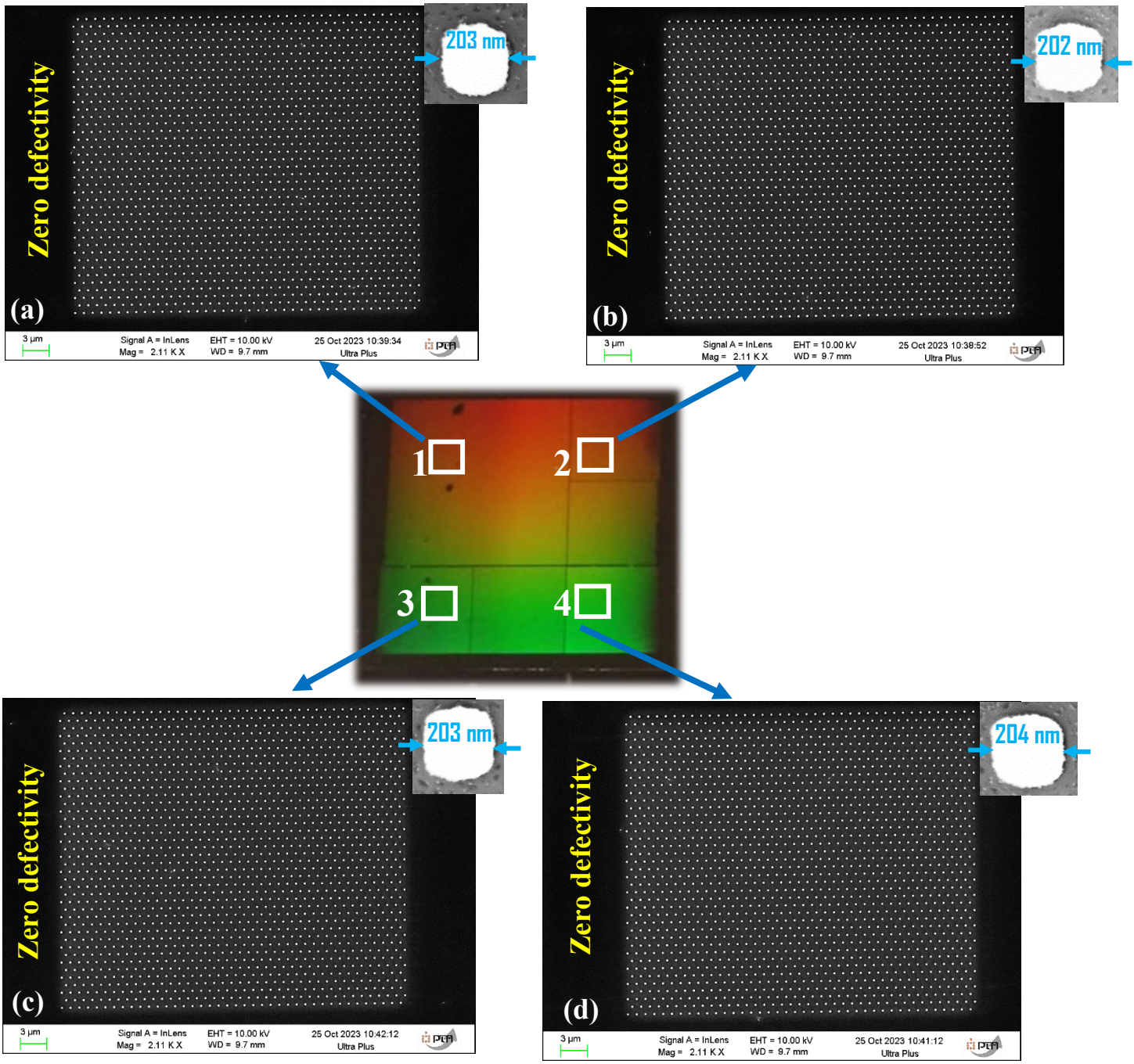

Figure 7. Zoomed views of nanopillar arrays and some measured diameters (a-d) from various zones 1-4 for 36x36 mm^2 etched surface.

All the nanopillars are standing up despite the bottom diameter reduction. Similarly, Figure 6-b demonstrates the formation of pillars measuring 200 nm in diameter at the top and 130 nm at the bottom SiO_2 with a pitch of 1 µm. The diameter reduction at the bottom of each nanopillar is an extremely crucial element in our strategy. This profile will facilitate the twisting of SiO_2-based nanopillars during GaN growth on the top of the nanopillars, thanks to the ability of SiO_2 to be deformed at the GaN growth temperature.[26,27] Once etching was finished, the sample was placed in a Cr-Etch solution for removing residues of the Cr etching mask.

The quality of the grown GaN material depends strongly on the quality of the primary array, since any missing pillar within the array can create a defect during the growth process. It is therefore absolutely necessary to control the patterning process in order to obtain arrays offering an ideal degree of homogeneity. Our initial focus was to investigate the defect rate on pillar arrays with a diameter of 200 nm. Figure 7 shows a uniform nanopillars diffraction image for the 36x36 mm^2 sample and its defect analysis on pillars having a nominal diameter of 200 nm at the top. Four areas were selected from the sample for defectivity investigations. SEM observations in Figure 7 a, b, c, and d showed that every selected zone had a complete array, with no missing pillar indicating excellent etching stability and zero defects. Concerning pillar diameters, the measurements revealed diameters of 200 nm $\pm$ 5 nm at the pillar top, which corresponds to the dimensions of the Si master. To check the accuracy of our approach, another defect characterization study was conducted. This study consisted of scanning 1000 positions in our sample with a pitch of 1 mm. As shown in figures 8-a, the statistics showed that we obtained a number of nanopillars varying between 100 and 97 in each array (a complete array contains 100 nanopillars). The defect histogram (figure 8-b) confirms that 90% of the arrays are complete with zero missing pillars. This study confirms that the defect rate of our approach is very low. Further measurements were performed and the same observations were revealed over the entire surface. These findings confirm the success of the used protocol in fabricating low defect nanopillar arrays on a 3x3 cm^2 surface, which will serve as the starting block for freestanding and easily transferable µLEDs.

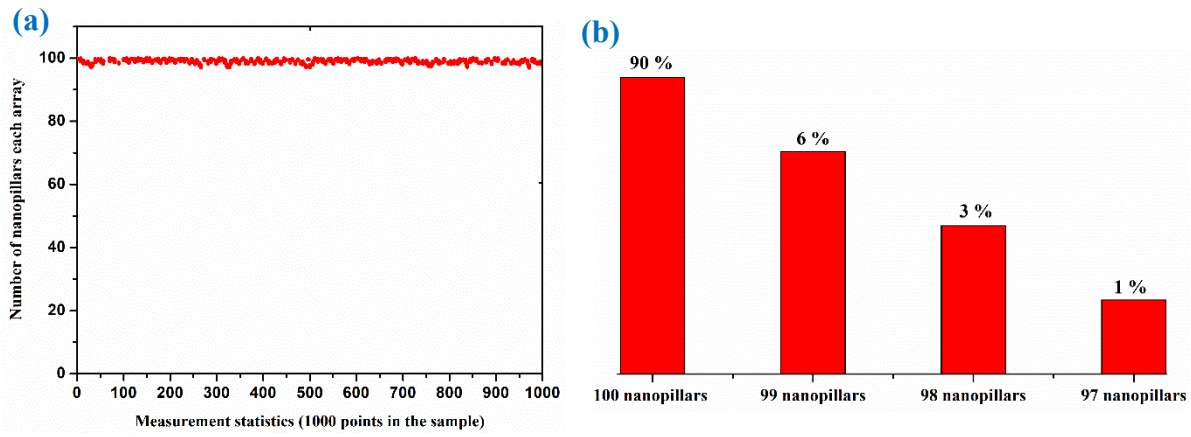

Figure 8. Defects characterization.

2.2 EDX analysis

Before the GaN growth, it was checked that there was no residual chrome on the top of the nanopillars in order to avoid any contamination. For this, the elemental composition of nanopillars, measuring 200 nm in diameter and etched 300 nm into the lower SiO_2 layer, was performed using EDX quantitative point analysis and mapping. Figure 9 shows the spectrum of the elemental composition and the individual mapping for each chemical element.

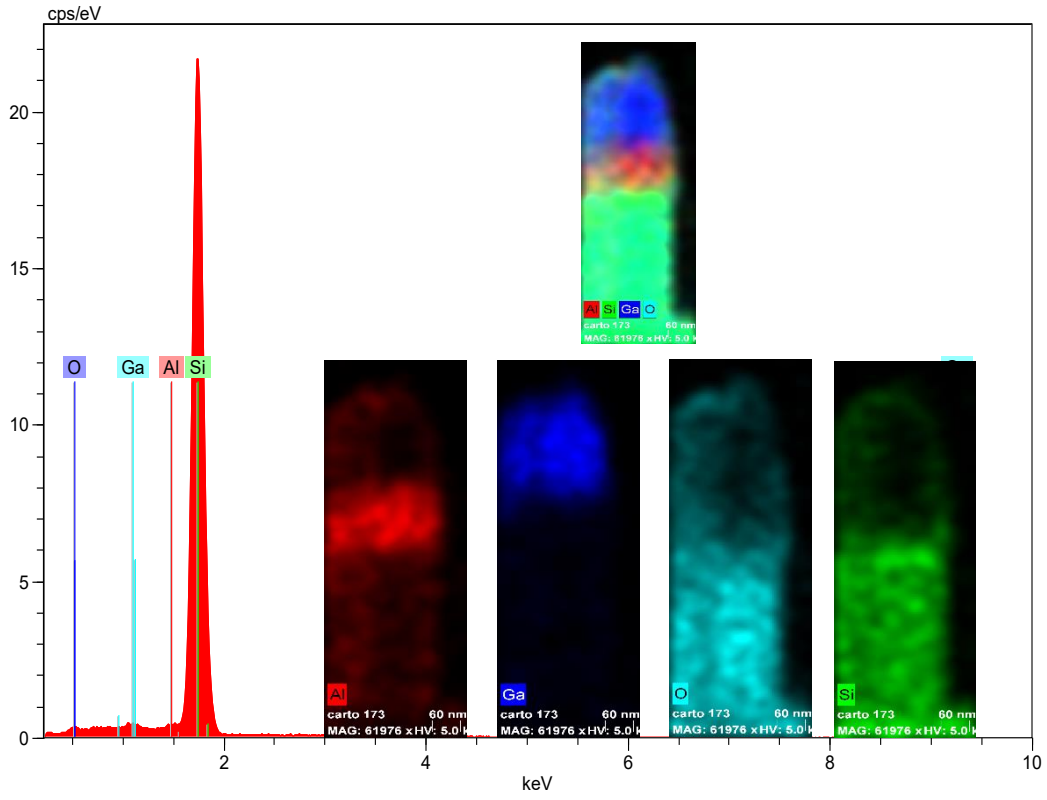

Figure 9. EDX analysis: elemental mapping for an etched 200 nm width pillar and its spectrum.

According to spectrum and individual mapping, we can clearly identify the 10 nm SiO_2 layer deposited on the GaN at the top of the pillar, as well as the other elements of the other layers. No Cr is detected in the spectrum and mapping, which confirms that 40 s in the Cr-Etch is sufficient to remove any remaining Cr hard mask.

2.3 Growth of high quality thick GaN on the top of the nanopillars

As mentioned before, the fabricated nanopillar arrays will be used for GaN and µLED structure growth. Figure 10-a illustrates the growth of GaN on top of SiO_2-based nanopillars. In this study, we have chosen to focus on nanopillars with 200 nm in diameter. The pendeoepitaxy of high quality thick GaN is conducted through two steps using trimethylgallium (TMGa) and ammonia (NH_3) as Ga and N source precursors, respectively, and H_2 as carrier gas. In the first step, 3D deposition at 950 °C, 100 Torr is carried out on the top of the nanopillars, forming a pyramid of GaN as shown by the top, zoomed out and cross sectional views in Figure 10 b-c. In this step, the top of the nanopillar behaves as an active growth site. Progressively, the pyramids coalesce through their lateral pyramidal facets.

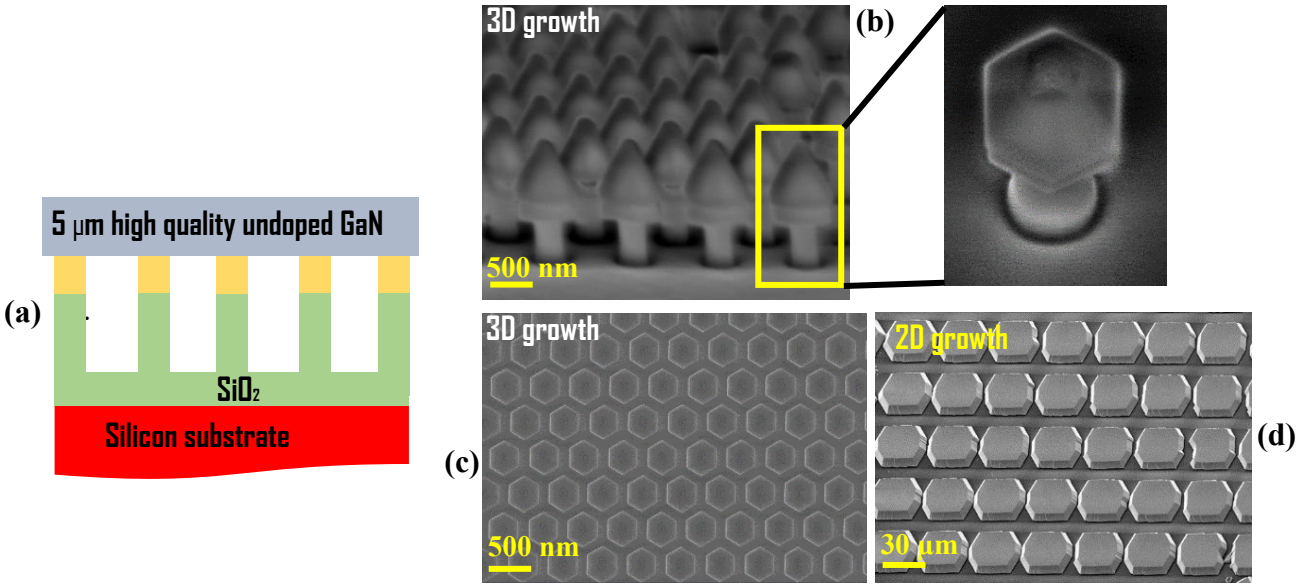

Figure 10. Growth of GaN platelets: (a) schematic of the grown GaN on the pillars, (b,c) 3D GaN growth on the top of the 200 nm pillars, (d) 2D GaN coalescence on the formed pyramids.

Subsequently, a 2D lateral deposition on the pyramids formed in the first step is processed at 1000 °C, 300 Torr in order to obtain a two-dimensional high quality GaN platelet as shown in Figure 10-d.

2.4 Epitaxial growth of µLED structure and its transfer towards carrier substrate

Figure 11 displays a schematic illustration of the µLED structure deposited on the two-step-formed GaN. This µLED structure consists of 1.5 µm of n-GaN, 3 alternating InGaN/GaN quantum wells, an electron blocking layer, 200 nm of p-GaN and a highly p^{++} GaN layer. The complete structure is shown in cross-sectional TEM in Figure 11-b, with a zoom on the QWs The growth of all these layers results in µLEDs formed on the NIL engineered nanopillars [29].

As mentioned in the introduction, one of the objectives of our bottom-up approach is to transfer µLEDs to solid or flexible substrates. In this context, surface roughness plays a significant role in such processes. A 2x2 μm^2 AFM scan of the µLED surface roughness was carried out, and figures 11-c and d demonstrate that the µLED surface is very smooth with an Rms of 0.6 nm.

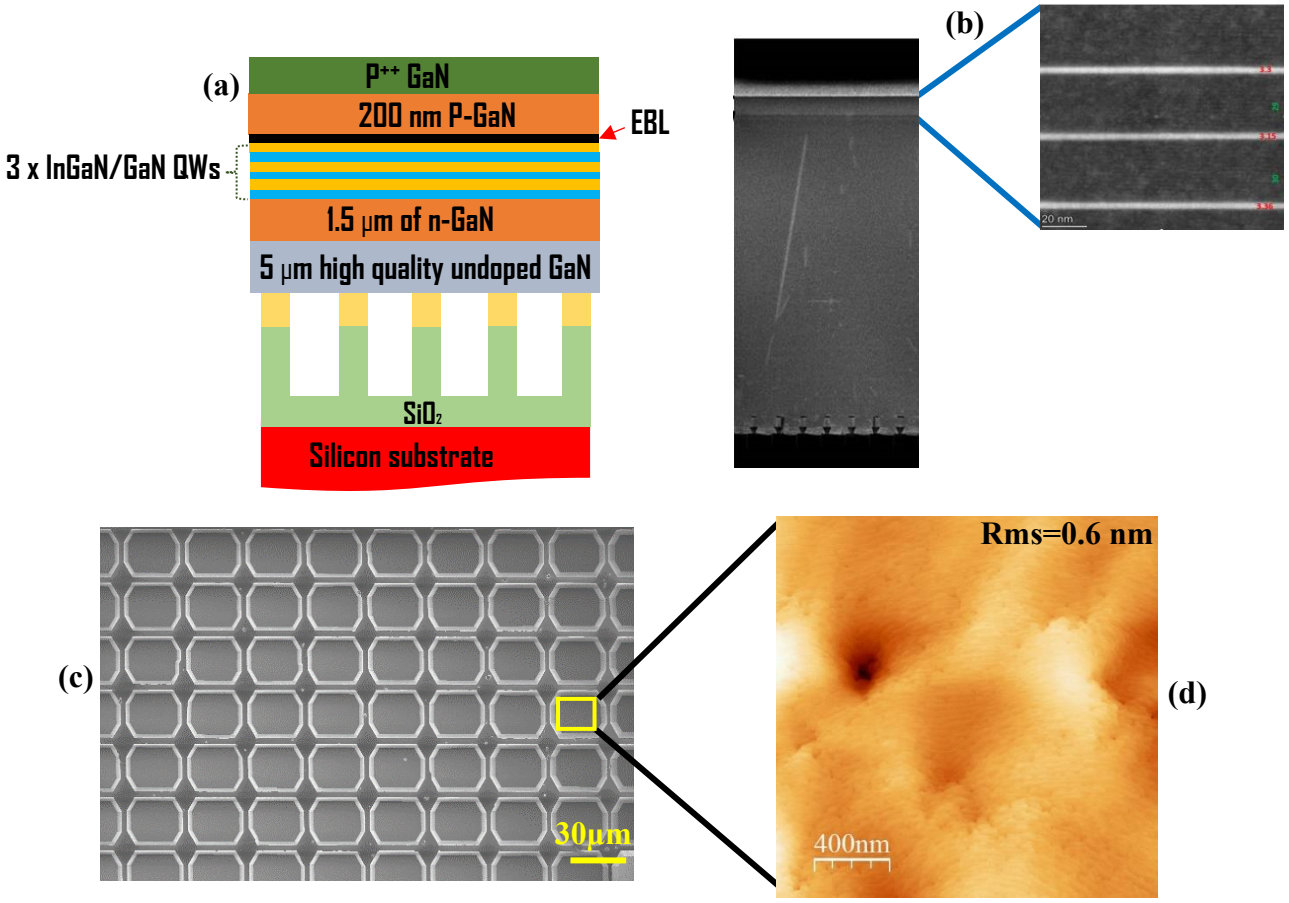

Figure 11. Epitaxial growth of µLEDs: (a) schematic illustration of the deposited µLED structure on pillars, (b) cross sectional TEM image of the grown µLED structure on GaN pillars and zoomed view of the 3 alternating InGaN/GaN QWs, (c) SEM top view of GaN-based µLEDs, (d) AFM image of the µLED surface.

Transferring µLEDs to a carrier substrate is one of the major challenges of active-matrix µdisplays. The carrier substrate onto which the GaN microLEDs are transferred in the current

study, a metal-coated Si substrate, mimics the CMOS active matrix that will precisely control the desired display µLED. According to the literature, various transfer methods can be used, including flip-chip bonding, transfer by printing, eutectic bonding, metal-metal bonding, laser and chemical debonding.[28-30] In our work, we have employed a strategy based on the combination of adhesive tape and metal-metal double bonding in order to enhance the transfer efficiency of µLEDs. The aim of this approach is to highlight a simple and effective transfer procedure. This method consists in first bonding the adhesive tape to the µLEDs then applying a homogeneous force in order to break the SiO_2-based nanopillars at the bottom of each µLED. Figure 12 shows µLEDs that have been partially collected by the adhesive tape, with a zoomed view showing the back of the µLED. This first part of the transfer is very helpful for getting maximum flexibility to manipulate the µLEDs and create any desired display design. In addition, these µLEDs can be transferred and bonded to a suitable substrate.

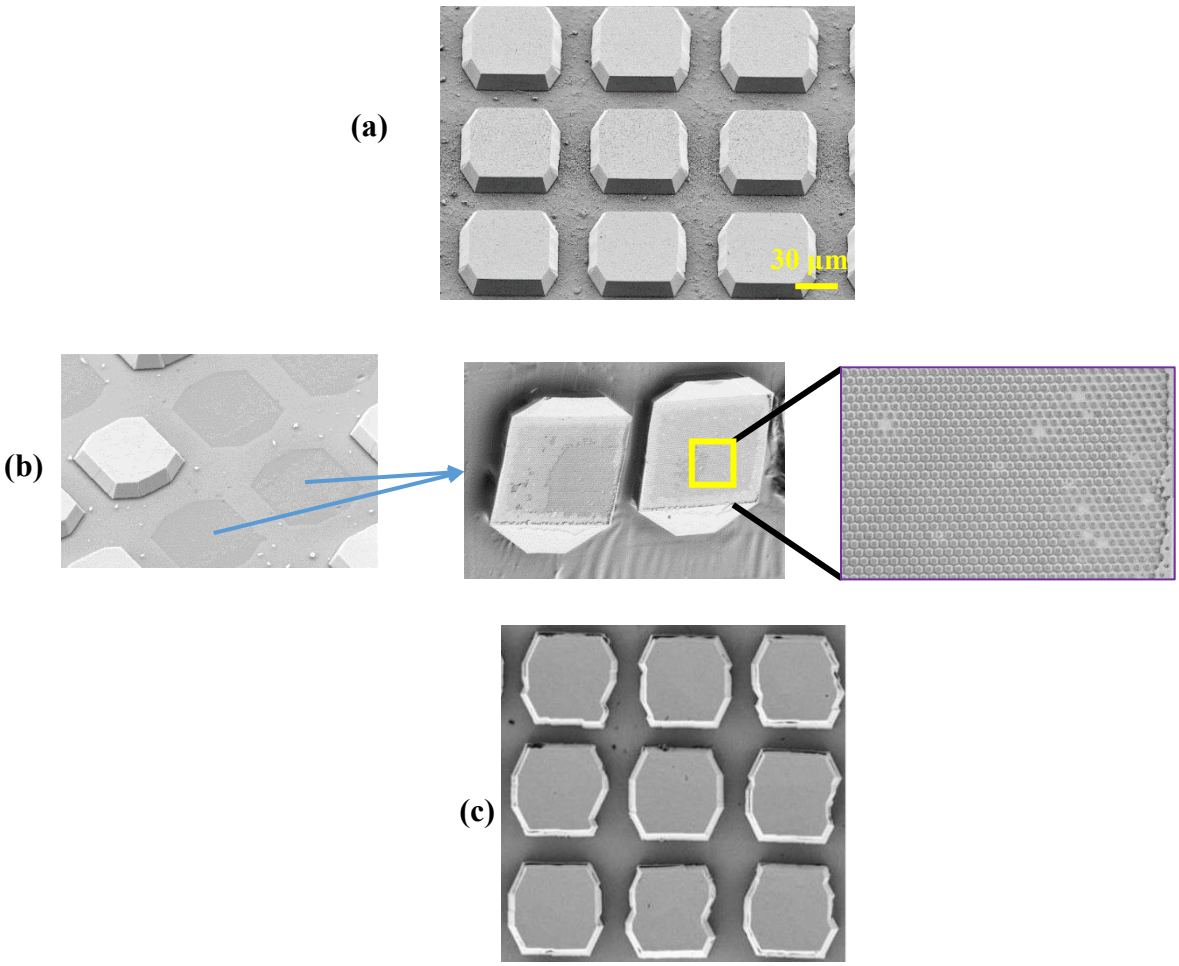

Figure 12. transfer of µLEDs: (a) SEM image of as-deposited µLEDs, (b) SEM images after partial transfer of µLEDs, (c) SEM image after total transfer of µLEDs to Si substrate.

For this purpose, a metal-metal bonding is adopted. This means that the µLEDs picked up on tape (Figure 12-b) before being coated with 150 nm of Tin (Sn), while 100 nm of gold is deposited on the Si substrate. Using thermocompression technique and optimizing several parameters such as temperature, pressure and annealing time, we succeeded to transfer the quasi-totality (90%) of µLEDs onto the Si substrate as shown in Figure 12-c. The findings described here and in the previous sections of the paper demonstrate the originality and novelty of our bottom-up approach based on the pendeoepitaxy of µLEDs on the top of 200 nm pillars. This solution offers excellent prospects for the fabrication of future generation µLED displays.

3. Conclusion

In this paper, we have established a µLED fabrication process using nano-imprint lithography without lift-off which is large scale and compatible with 200mm silicon photonics platform. For this, a nanopatterning and transfer protocol have been optimized onto GaN on SOI substrates via NIL. Afterwards, the established no-liftoff approach was applied to fabricate GaN/AlN/Si/SiO_2/Si nanopillars by plasma etching. The resulting nanopillars feature a special profile and a bottom SiO_2 diameter smaller than that of the top. This finding is highly advantageous for promoting the twisting of SiO_2 and thus reducing the dislocation density within the grown GaN. In addition, the developed approach provides nanopillar arrays without defects or missing pillars, and with pillars having diameters of 100 and 200 nm. As a result, freestanding µLEDs were successfully formed on top of nanopillars using a bottom-up approach. AFM scans showed the smoothness of the µLED surface, and these µLEDs were easily transferred onto a silicon substrate by combining adhesive tape and metal-metal bonding steps.

4. Experimental Section

The experimental and fabrication details of nanopillars are illustrated in Figure 1. In this section, an overview of the tools and settings involved in each phase is outlined.

GaN on SOI epitaxy:

The GaN-based structure stack used in the present study consists of several layers of materials grown on an SOI substrate formed by bulk Si, 400 nm SiO_2 and 45 nm Si. On top of the SOI, a 100 nm AlN layer is grown to avoid melt back etching and interface defects between the Si and the 160 nm of GaN which is grown on top. The layers are grown by metal organic vapor phase epitaxy (MOVPE) in an AIXTRON close-coupled showerhead (CCS) reactor using trimethylaluminium(TMAl), trimethylgallium (TMGa) and ammonia (NH_3) as precursors. A

10 nm layer of SiO_2 PVD is deposited on the GaN for masked pendeopepitaxy in the subsequent steps, as detailed in our previous publication on the growth method.[23]

Si master fabrication, antisticking treatment, PDMS mold:

For the nanopatterned surface, the nanostructuration of a 36x36 mm^2 surface of Si substrate was conducted on a Vistec SB0354 electron beam lithography (EBL) machine using a NEB22 resist annealed at 110 ºC and its corresponding MF21A developer. Then, the patterns were transferred to Si by dry etching via 50 nm SiO_2 as hard mask using different plasmas based on CF_4, CL_2, He-O_2, HBr gases within an Applied Materials Centura Etch reactor. Then, an antisticking treatment by depositing a 1H,1H,2H,2H-Perfluorooctyltriethoxysilane (FDTS) thin layer is conducted in order to render the Si master surface highly hydrophobic and facilitate the demolding of the cured PDMS mold. This flexible mold is prepared from the FDTS Si master and is ready for NIL patterning experiments.

NIL patterning:

NIL patterning experiments, for the nanotransfer of mold dimensions into mr6000 resist surface, have been carried out using an EITRE6 Obducat tool using a pressure of 1 bar and temperature of 75 ºC.

Etching:

After the nanotransfer by NIL, a 200 mm Applied Materials Centura Etch reactor is deployed for transferring the imprinted patterns through the resin and the SiO_2/Cr hard masks and then to the GaN layers using our no-liftoff approach via several different plasmas. The etching tracking of each material is conducted using an end-point system of VERITY INSTRUMENTS EYE-D spectrograch.

Regrowth of GaN and µLED structure:

The ~5µm thick GaN platelet was deposited in two main steps on the top of the nanopillars followed by the growth of the µLED structure which consists of a Si-doped n-GaN layer followed by InGaN/GaN multi-quantum wells, an AlGaN electron blocking layer and a Mg-doped p-GaN top layer.[23]

Characterization

Scanning electron microscopy (SEM): The nanopillars were observed, analyzed and mapped at high resolution using a Zeiss SEM equipped with an EDS detector operating at 10kV acceleration voltage.

Atomic force microscopy (AFM): The μLED topography and surface roughness were examined using a Veeco dimension III AFM in tapping mode.

Acknowledgments

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Conflict of Interest

The authors declare no conflict of interest.

Keywords

nanoimprint lithography, plasma etching, GaN nanopillars, zero defectivity, pendeoepitaxy, μLEDs.

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