Special Session: On-chip jitter BIST with sub-picosecond resolution at GHz frequencies

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***Abstract*—This paper describes an on-chip instrument for jitter estimation of clock signals in the GHz range with a sub-picosecond resolution. A self-referenced technique is used to remove the need of a very clean external reference clock. The instrument has been designed in STMicroelectronics 28 nm FDSOI technology. By exploiting the fine delay control which can be achieved with this technology, simulation results haven shown a resolution down to 100 fs for GHz clock signals with a simple calibration procedure.**

I. Introduction

Clock jitter is the deviation of a clock edge relative to a reference time frame. In the current age of high speed communication and I/O systems, clock jitter impacts the system performance. With increased data transfer rates, measuring clock jitter in the sub-picosecond range is becoming necessary. Jitter measurement with this level of resolution during production testing or through prototyping design stages needs high-speed oscilloscopes or spectrum analyzers which are also often expensive. On-chip jitter measurement offers a low-cost solution that also overcomes the inaccuracies in measurement that arise due to RLC effects while tapping high speed clocks for off-chip measurement.

On-chip jitter measurement techniques can be classified into two main categories that include, on one hand, the use of an external clock reference and, on the other hand, self-referenced techniques. The first category includes conventional techniques that use a clean reference and are often based on coherently undersampling the Signal Under Test (SUT) with the external clock.

Jitter estimation techniques that remove the need of an external reference clock are the second category of on-chip instruments and are generally termed as self-referenced techniques. These measurement schemes use a delayed version of the SUT to sample the clock itself to extract the jitter [1]. Self-referenced techniques for on-chip jitter measurement have been experimentally demonstrated with a resolution of 400 fs in [2], and 300 fs later in [3], for signals up to a few GHz. A resolution below 100 fs has been shown experimentally in [4], but with signals below 1 GHz with the use of a time-difference amplifier.

A self-referenced technique for random jitter estimation uses delay lines to sample the clock under test with a delayed version of itself at various instants of time in the vicinity of the expected clock edge. The probability that a given edge leads or lags its delayed version gives rise to a jitter histogram from which RMS jitter is computed [1]. This work proposes an implementation of a jitter test instrument using self-referenced technique in 28 nm FDSOI using the fine delay control achievable with this technology and demonstrates the feasibility of sub-picosecond resolution for clock jitter measurement in the GHz range.

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II. A self-referenced jitter BIST

Fig. 1 shows the block diagram of the jitter test instrument using the self-referenced technique. This instrument has first an NT delay block to delay the SUT. This block is composed of a cascade of delay elements of the type described in [5] where N is the number of delayed periods and T the period of the SUT. The NT delayed clock acts as the sampling clock for the SUT. As demonstrated in [4], by setting the NT delay to multiples of the clock period, the jitter correlation between both signals will be very low (at least for random jitter) and the absolute jitter of the SUT can be extracted with a gain of $\sqrt{2}$ from the N-period jitter that is measured by construction.

The Time Difference Amplifier (TDA) amplifies the time difference between the SUT and the sampling clock, thereby expanding the resolution of measurement by its gain. The SUT and sampling clock next traverse a Vernier Delay Line (VDL) made of a cascade of Vernier delay cells, each biased for a delay $Gain_{TDA} \times \Delta$, where Δ is the target jitter resolution of 100 fs and the TDA gain is approximately 100. The Vernier delay cells are made of the same type of delay elements as for the NT delay. The sampling clock is incrementally delayed after each Vernier delay cell in the line. A phase comparator is used at the output of each VDL cell to detect the lead or lag of the SUT with respect to its delayed version. A counter stores the number of hits at the output of each VDL cell and this is used to generate the histogram.

The principle for the generation of the jitter histogram is illustrated in Fig. 2 for a VDL that contains 25 delay cells. The outputs of each VDL cell allow computing one point of the Cumulative Distribution Function (CDF) of the jitter, at regular delays in the vicinity of the expected clock edge of the SUT. For each delay cell, the SUT is processed for a fixed time-length in order to produce the value of the corresponding CDF bin that is scanned out from the chip. The calculated bin values are assembled to produce the CDF. The jitter PDF is obtained off-chip by derivation of the CDF, and the absolute RMS jitter is calculated from it after correction by a factor of $\sqrt{2}$. It must be noticed that the implementation only considers sampling

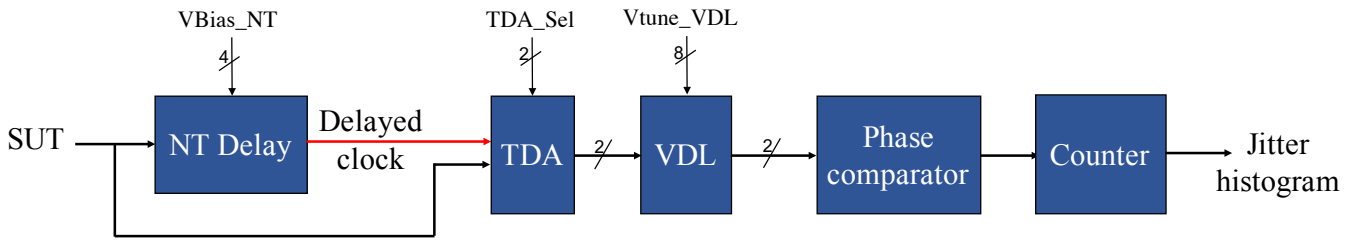

Fig. 1. A self-referenced jitter BIST

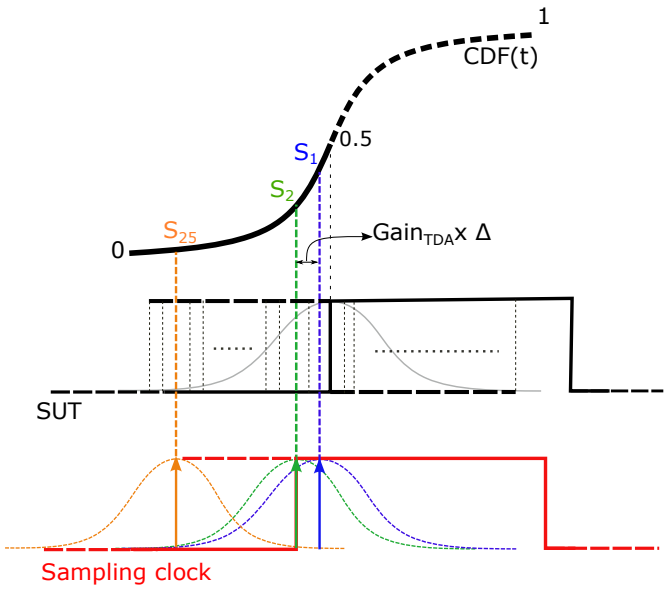

Fig. 2. Generation of jitter CDF

one side of the SUT random jitter PDF that is considered symmetrical.

III. Simulation Results

Simulation results have been obtained with a transistor level transient noise simulation of the instrument described in Fig. 1 with the counter and digital control circuitry modeled at higher level in Verilog-A. These Spectre simulations are extremely time consuming and often require few weeks of run time and implementing the digital circuitry that supports the programmability of the instrument in Verilog-A saves run time. The jitter histogram generated with a SUT frequency of 1 GHz is shown in Fig. 3. The vertical axis shows the number of hits for each of the bins in the histogram. These hits were obtained by simulating each bin for 1500 clock cycles. An RMS random jitter of 0.8 ps has been injected in the input clock signal. Post-processing of the obtained jitter histogram results in an measured RMS jitter estimate of 0.7 ps which shows a resolution of 100 fs.

IV. Conclusions

This paper has presented an implementation of an on-chip jitter BIST in 28 nm FDSOI with simulation results

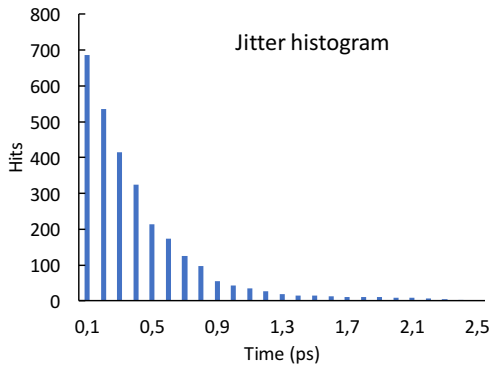

Fig. 3. Jitter histogram for 1 GHz clock frequency

that demonstrate the feasibility of a sub-picosecond resolution for jitter estimation for clocks up to 1 GHz. The FDSOI technology provides advantages due to tunability and low noise to reach a high resolution with simple calibration as described in [6]. A highly tunable delay element along with a TDA supports a sub-picosecond resolution of clock jitter measurement for frequencies in the GHz range.

Acknowledgements

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