Special Session: A high-frequency sinusoidal signal generation using harmonic cancellation

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***Abstract*—An on-chip high-frequency sinusoidal signal generator with a calibration circuit based on a coarse-fine delay cell is presented in this work. The harmonic cancellation principle is used for signal generation by adding scaled and time-shifted versions of a periodic signal. However, as the output frequency increases in the GHz range, the harmonic cancellation can be severely affected by non-idealities such as mismatch and variations on timing parameters (phase difference, duty cycle) of the time-shifted signals. This degrades the spectral purity of the output signal. To counter this, a calibration circuit based on a coarse-fine delay cell is integrated into the system to correct the timing parameters of the signal. Simulation results show a THD better than −60 dB in the frequency range from 500 MHz to 2 GHz.**

I. Introduction

The use of Built-In Self-Test (BIST) for Analog, Mixed-Signal, and RF (AMS-RF) circuits is one of the solutions to improve yield in advanced nanometric processes. BIST circuits allow the characterization of internal blocks in highly integrated SoCs and SiPs and avoid the use of expensive AMS-RF testers. Moreover, advanced features like calibration and in-field testing in safety-critical applications can be enabled via AMS-RF BIST. In a wide variety of AMS-RF tests, a key element is the test stimulus generator. In particular, many analog test strategies are based on applying a sinusoidal signal with a high spectral quality as a test stimulus. Therefore, on-chip sinusoidal signal generation can be identified as a key point for enabling AMS-RF BIST. In this regard, signal generators based on the harmonic cancellation principle have been extensively explored because they offer a highly linear output signal with reduced on-chip resources, in some cases mostly relying on digital circuits [1]–[12].

The harmonic cancellation process linearizes a periodic signal by combining time-shifted and scaled versions of the original periodic signal [13]–[15]. Since the generation of digital square-wave signals is simple compared to other types of periodic signals, square-wave signals are considered in the paper. There can be multiple ways by which different combinations of the time-shifted square waves and their scalar weights can be chosen to cancel a certain number of harmonics [10]. A practical solution that represents a good trade-off consists of five signals that are time-shifted by $\pm\frac{\pi}{6}$ or $\frac{T}{12}$ and the scalar weights by which these signals should be scaled are $\frac{\sqrt{3}}{2}$, $\frac{1}{2}$, and 1 as shown in Fig. 1. This solution cancels all odd harmonics below the 11^{th} harmonic assuming a $50\,\%$ duty cycle for ensuring that no even harmonics are present in the output signal. Higher-order harmonics can be attenuated with the help of a lenient low-pass filter.

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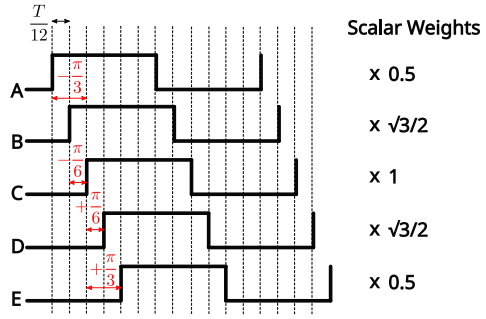

Fig. 1. Ideal timing diagram for harmonic cancellation.

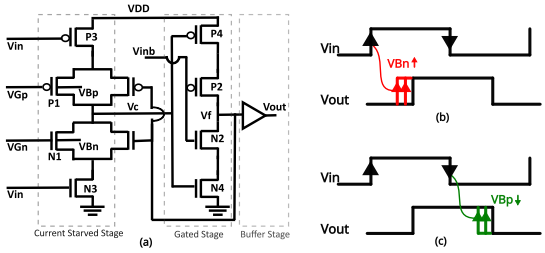

Fig. 2. (a) Coarse-fine delay cell. (b) Phase change due to change in VBn. (c) Duty cycle change due to change in VBp

II. Timing Inaccuracies in High Frequency and Their Mitigation

Advanced fabrication processes come with non-idealities such as mismatch and process variation. These non-idealities can affect the timing properties of square waves and the scalar weights that affect the efficiency of the harmonic cancellation and can severely degrade the quality of the generated output signal. For low-frequency applications, the quality is mainly limited by the mismatch in scalar weights while in high-frequency applications timing errors are responsible for the quality of the output signal [10]. Some solutions are proposed in [1]–[5], [10] but these solutions are either limited to low-frequency signals or limited by the resolution by which these timing issues can be corrected. To address these limitations, in this work we make use of a coarse-fine tunable delay cell that takes advantage of the back bias capabilities of FD-SOI technology [16] as shown in Fig. 2(a). The phase of the signal can be corrected by changing the body voltage (VBn) of transistor N1 as shown in Fig. 2(b) while the duty cycle is corrected by changing the body voltage (VBp) of transistor P1 as shown in Fig. 2(c).

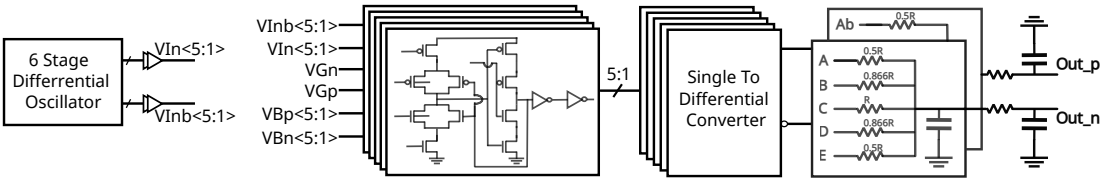

Fig. 3. Conceptual block diagram of the proposed sinusoidal signal generator with calibration.

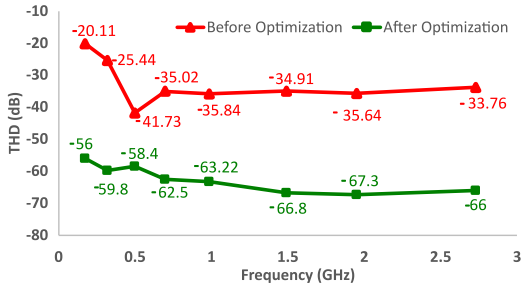

Fig. 4. THD of the generated signal before and after optimization as a function of the output frequency.

III. Practical Implementation and Results

The architecture of the sinusoidal signal generator with timing calibration is shown in Fig. 3. The square-wave signals are generated from a 6-stage fully-differential ring oscillator. These signals are passed through a buffer stage and the output of the buffer stage is then fed to the coarse-fine delay cells for correction of timing errors. The output of each delay cell is connected to a single-to-differential signal converter that generates differential signals. The outputs of the single-to-differential stage are scaled and added using a weighted RC network followed by a low pass filter that attenuates the higher-order harmonics. The complete system has been implemented using STMicroelectronics 28 nm FD-SOI technology. The values of the control voltages in the coarse-fine delay cell are optimized to minimize the THD of the generated output signal. Fig. 4 shows the THD as a function of the frequency of the output signal before (red) and after (green) optimization of the control voltages, for frequencies ranging from 173 MHz to 2.73 GHz. For frequencies greater than 500 MHz, the THD of the generated signal is consistently better than -60 dB.

IV. Conclusions

A harmonic cancellation-based sinusoidal signal generator with calibration of timing errors using a coarse-fine delay cell is proposed in this work. Simulation results show that the timing errors (phase mismatch and duty cycle error) at higher frequencies are corrected with the help of a coarse-fine delay cell that overcomes the limitations of previously proposed solutions. A THD better than -60 dB can be achieved for a wide range of output frequencies from MHz to GHz.

Ackowledgements

This work has been carried out in collaboration with STMicroelectronics within the Nano2022 research program.

References

[1] B. Karthik Vasan, S. K. Sudani, D. J. Chen, and R. L. Geiger, "Low-distortion sine wave generation using a novel harmonic cancellation technique," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 60, no. 5, pp. 1122–1134, 2013.

[2] M. J. Barragan, G. Leger, D. Vazquez, and A. Rueda, "On-chip sinusoidal signal generation with harmonic cancellation for analog and mixed-signal BIST applications," *Analog Integrated Circuits and Signal Processing*, vol. 82, no. 1, pp. 67–79, 2015.

[3] P. Aluthwala, N. Weste, A. Adams, T. Lehmann, and S. Parameswaran, "Design of a digital harmonic-cancelling sine-wave synthesizer with 100 MHz output frequency, 43.5 db SFDR, and 2.26 mW power," in *2015 IEEE International Symposium on Circuits and Systems (ISCAS)*, 2015, pp. 3052–3055.

[4] P. D. Aluthwala, N. Weste, A. Adams, T. Lehmann, and S. Parameswaran, "Partial dynamic element matching technique for digital-to-analog converters used for digital harmonic-cancelling sine-wave synthesis," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 64, no. 2, pp. 296–309, 2017.

[5] C. Shi and E. Sánchez-Sinencio, "150–850 MHz high-linearity sine-wave synthesizer architecture based on fir filter approach and sfdr optimization," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 62, no. 9, pp. 2227–2237, 2015.

[6] ——, "On-chip two-tone synthesizer based on a mixing-fir architecture," *IEEE Journal of Solid-State Circuits*, vol. 52, no. 8, pp. 2105–2116, 2017.

[7] H. Malloug, M. J. Barragan, S. Mir, L. Bastères, and H. Le Gall, "Design of a sinusoidal signal generator with calibrated harmonic cancellation for mixed-signal bist in a 28 nm fdsoi technology," in *2017 22nd IEEE European Test Symposium (ETS)*, 2017, pp. 1–6.

[8] H. Malloug, M. J. Barragan, and S. Mir, "Practical Harmonic Cancellation Techniques for the On-Chip Implementation of Sinusoidal Signal Generators for Mixed-Signal BIST Applications," *Journal of Electronic Testing: Theory and Applications*, vol. 34, no. 3, pp. 263–279, 2018.

[9] ——, "A 52 db-SFDR 166 MHz sinusoidal signal generator for mixed-signal bist applications in 28 nm fdsoi technology," in *2019 IEEE European Test Symposium (ETS)*, 2019, pp. 1–6.

[10] A. Mamgain, M. J. Barragan, and S. Mir, "Analysis and mitigation of timing inaccuracies in high-frequency on-chip sinusoidal signal generators based on harmonic cancellation," in *2021 IEEE European Test Symposium (ETS)*, 2021, pp. 1–6.

[11] G. G. Garayar-Leyva, H. Osman, J. J. Estrada-López, and E. Sánchez-Sinencio, "A harmonic-canceling synthesizer using skew-circulant-matrix-based coefficient generator," in *2020 IEEE International Symposium on Circuits and Systems (ISCAS)*, 2020, pp. 1–5.

[12] G. G. Garayar-Leyva, H. Osman, J. J. Estrada-López, and O. Moreira-Tamayo, "Skew-circulant-matrix-based harmonic-canceling synthesizer for bist applications," *Sensors*, vol. 22, no. 8, 2022. [Online]. Available: https://www.mdpi.com/1424-8220/22/8/2884

[13] E. Mensink, E. A. M. Klumperink, and B. Nauta, "Distortion cancellation by polyphase multipath circuits," *Circuits and Systems I: Regular Papers, IEEE Transactions on*, vol. 52, no. 9, pp. 1785–1794, Sept. 2005.

[14] E. Seok, C. Cao, D. Shim, D. J. Arenas, D. B. Tanner, C.-M. Hung, and K. K. O, "A 410GHz CMOS push-push oscillator with an on-chip patch antenna," *Solid-State Circuits Conference, 2008. ISSCC 2008. Digest of Technical Papers. IEEE International*, pp. 472–629, 3-7 Feb. 2008.

[15] Y.-L. Tang and H. Wang, "Triple-push oscillator approach: theory and experiments," *Solid-State Circuits, IEEE Journal of*, vol. 36, no. 10, pp. 1472–1479, Oct 2001.

[16] S. Clerc, T. Di Gilio, and A. Cathelin, *The Fourth Terminal: Benefits of Body-Biasing Techniques for FDSOI Circuits and Systems*. Springer, 2020.