Nonintrusive Machine Learning-Based Yield Recovery and Performance Recentering for mm-Wave Power Amplifiers: A Two-Stage Class-A Power Amplifier Case Study

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***Abstract*—State-of-the-art nanometric fabrication processes enable the integration of monolithic millimeter-wave (mm-wave) circuits. However, nanometric technologies are prone to process variations that may significantly impact the performance of the fabricated mm-wave circuits and dramatically reduce the fabrication yield. In order to improve the fabrication yield, extensive resources are required for tuning the functionality of each fabricated die in the production line, especially in the mm-wave domain. In this work, we implement and experimentally validate a machine learning-based calibration strategy for mm-wave circuits that significantly simplifies this tuning process. A machine learning algorithm is employed to predict the optimum values of a set of on-chip tuning knobs based on nonintrusive measurements provided by embedded process monitor circuits. The proposed technique is demonstrated on a 69 GHz power amplifier with one-shot calibration capabilities integrated in STMicroelectronics 55 nm CMOS technology. Experimental results on a set of 39 fabricated samples demonstrate the feasibility and performance of the proposed machine learning-based calibration for yield recovery and performance recentering applications.**

***Index Terms*—Machine learning-based calibration, machine learning-based test, mm-wave integrated circuits, power amplifiers, yield enhancement.**

I. Introduction

NOWADAYS, the constant evolution of nanometric integrated technologies with optimized Back-End-Of-Line (BEOL) metal stacks allows the development of high-performance monolithic mm-wave circuits. This evolution is guided by the needs of a wide variety of applications such as high data-rate communications, healthcare imaging systems, automotive radar, etc. Monolithic mm-wave integration in conventional silicon technologies has the clear advantage of reducing the cost and enabling the co-integration with complex VLSI systems including analog, mixed-signal, and digital functions. However, at the same time, integrating mm-wave circuits in advanced nanometric technologies creates new challenges. Nanometric technologies are prone to process variations that may dramatically degrade the performance of sensitive RF and mm-wave circuits [1], [2]. Additionally, mm-wave circuits often include full-custom passive elements which may complicate evaluating the impact of process variations at the design stage. As a consequence, fabrication yield may be significantly limited, especially for safety-critical applications with stringent performance requirements.

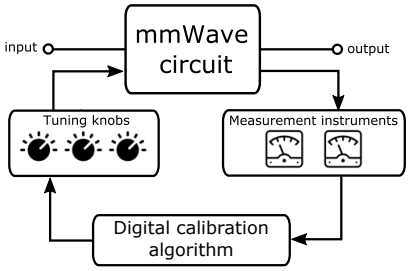

Fig. 1. General scheme of an RF/mm-wave calibration strategy.

Improving the fabrication yield is a major concern for the IC industry that may be addressed in several ways. Simply overdesigning the RF and mm-wave circuits to increase robustness is not usually a viable option due to the excessive area and power overheads that it may require. Design-enabled solutions targeted at the mitigation of process variations exist, but they are usually limited to a given circuit architecture or to particular circuit families [3]. A more general and common solution is to add some embedded calibration capabilities to be able to calibrate the design, should an excessive deviation with respect to the design target occurs [4]–[20]. Moreover, adding calibration capabilities to a mm-wave circuit has the additional advantage of enabling the reuse of the circuit in different applications within the tuning range of the circuit,

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which may open the door to reusable multi-purpose IPs that could be re-tuned to address different application scenarios requiring different performance trade-offs.

A general scheme for such a calibration strategy is represented in Fig. 1. In essence, a calibration strategy comprises some performance measuring capabilities and/or appropriate tunable elements (usually called tuning knobs), in such a way that it is possible to a) evaluate the actual performance of the circuit, and b) tune the performance of the circuit according to a predefined design target. An optimization algorithm oversees the calibration process by reading the performance measurement and searching for the optimum position of the tuning elements to comply with the given target performance.

In this work, we implement and experimentally demonstrate a calibration technique for mm-wave integrated circuits. The developed technique comprises a machine learning-based calibration scheme based on the use of on-chip nonintrusive process monitors and one-shot calibration techniques. The proposed machine learning-based one-shot calibration brings the advantages of:

1) *Not requiring direct performance measurements to guide the calibration process.* mm-wave direct measurements are costly, time-consuming, and highly subject to imprecisions. Instead, we propose to employ on-chip nonintrusive process monitor circuits to generate DC and low-frequency indirect signatures sensitive to process variations. These process signatures are specially designed to be highly correlated to the circuit's at-speed performance. After a training process in which direct performance measurements and nonintrusive signatures are measured for a reduced subset of devices, a predictive model is obtained allowing to guide the calibration based only on the measurement of the sensor signatures. Notice that the training set will always be small in regard to the production volume. The performance measurements can thus be performed using dedicated high-performance test equipment and boards, which are orders of magnitude cheaper than high-end Automated Test Equipment (ATE) for the production line [21]. The process monitor circuits are not connected or coupled to the device under calibration, which also reduces the design complexity.
2) *Avoiding the need of test-and-tune iterations.* The optimum position of the tuning knobs is predicted by a machine learning algorithm from the set of nonintrusive signatures, without the need for lengthy iterative calibration loops.

This paper is an extension of our previous conference paper [4]. This previous publication outlined the basic concepts of one-shot statistical calibration based on nonintrusive process monitors and offered a preliminary demonstration of a yield enhancement application based on electrical simulations of a power amplifier with built-in calibration capabilities. The present manuscript expands our previous work in multiple areas. Firstly, the scope of the proposed application has been extended beyond yield enhancement. In this new manuscript, we explore the capabilities of the proposed one-shot tuning strategy for performance recentering and for exploring performance trade-offs, based on a machine learning-based generation of the circuit's sample-dependent Pareto-optimal fronts. Then, considering a case study implementation to guide the discussion, the theoretical content of the paper has been expanded to cover extensively the basis of the proposed methodology and its practical implementation, including the design of the tuning knobs, the selection of process monitor circuits, and the implementation and training of the machine learning-based calibration model. Additionally, generic methodological guidelines to extend the proposed technique to other power amplifier architectures are detailed. Finally, the described proof-of-concept case study has been fabricated and fully characterized in the laboratory to experimentally demonstrate the feasibility of the proposed yield enhancement and performance recentering techniques. A critical comparison to the existing state-of-the-art is also presented to put our results into perspective.

The manuscript is organized as follows. Section II reviews briefly the existing literature on RF and mm-wave integrated circuits with embedded calibration and presents the key elements of our proposal within this context. In Section III we describe the theoretical basis of our calibration algorithm, including the statistical one-shot calibration approach and the proposed nonintrusive performance monitoring. Section IV presents the complete design of a 2-stage class-A 69 GHz PA with embedded calibration in STMicroelectronics 55 nm CMOS technology, including a generic tuning knob based on programmable decoupling capacitors and dedicated process control monitors to guide the calibration algorithm. Detailed guidelines are also provided to extend the proposed methodology to other architectures, implement the machine learning calibration algorithm and define an appropriate training set. Section V experimentally demonstrates the feasibility and performance of the proposed calibration on a set of 39 fabricated PA samples. Two calibration scenarios are considered: a nominal calibration aimed at improving fabrication yield and an aggressive calibration aimed at exploring different performance trade-offs. Finally Section VI summarizes our main contributions.

II. Previous Works

Initial works on embedded calibration for RF and mm-wave circuits focus on simplifying complex RF and mm-wave performance measurements, usually based on some built-in test capabilities to guide an iterative calibration algorithm, while tuning capabilities are usually provided by varying the bias conditions of the circuit. Thus, the work in [5] presents a classical test-and-tune calibration method for an integrated 8-18 GHz receiver. A set of on-chip ring oscillators is employed to excite the different elements in the receiver, whereas external test equipment is employed for monitoring the receiver's performance. Tuning capabilities are achieved by programming the bias currents and bias voltages of the LNA and mixer in the receiver.

A power detector for non-invasive calibration of differential PAs is presented in [6]. The power detector takes advantage

of a dedicated output transformer designed to provide output matching, differential-to-single-ended transformation, and, thanks to the addition of a third extra winding, power sensing capabilities. The work in [7] presents a load-insensitive PA that employs a six-port reflectometer to monitor load mismatch. A test-and-tune iterative algorithm is then employed to find the optimum values of the PA power supply and input drive and to tune a varactor in the matching network. The system is demonstrated in a 900 MHz PA integrated on a PCB.

In the same line, the work in [8], [9] proposes a set of embedded test instruments for on-chip calibration purposes. In particular, a VCO and a peak detector for exciting and acquiring, respectively, the output response of a 1.57 GHz LNA. In this case, the calibration algorithm is based on a machine learning regression that predicts the best bias and power supply conditions based on the output of the peak detector.

The calibration strategy in [10] is also based on a machine learning algorithm. In this case, an embedded envelope detector is employed for predicting the performance of a 1.9 GHz LNA from the response to an externally applied optimized stimulus. Two dedicated tuning knobs are presented: a bias voltage and a PMOS IMD sinker that is specially tailored to the architecture of the LNA under study. The proposed approach is further extended in [11] for the calibration of complete RF front-ends using the bias and supply of the different building blocks as tuning knobs.

Data-driven techniques for calibration are also explored in [12], [13]. Thus, the approach in [12] explores the application of reinforcement learning algorithms in the context of performance control and calibration of mm-wave Doherty PAs. The work in [13] explores the application of Bayesian Model Fusion to improve the performance of a calibration loop. The proposed technique is demonstrated in a 25 GHz VCO with a phase noise calibration loop based on monitoring indirect performances such as current consumption, oscillation frequency, and oscillation amplitude.

The approach in [14] employs nonintrusive process variation monitors, initially proposed in [15] for yield enhancement and calibration of mixed-signal circuits, in a machine learning-based calibration loop for a 2.4 GHz PA. The bias voltages and power supplies act as the tuning knobs. This is a limitation that is common to most of these early works on machine learning-based calibration: the key element for tuning the performance is the power supply of the device under calibration. From a system-level design point of view, the required control on the power supply, in addition to impacting the signal dynamic range, would imply a deep re-design of the power management circuit that may increase the complexity of the system, degrade the system's performance and create reliability risks if multiple power domains are required.

To avoid power supply tuning, other works are focused on novel design solutions for tunable elements suitable for RF and mm-wave circuits. Thus, a tapped gate inductor is proposed in [16] to calibrate the input matching of a 1.9 GHz LNA. The measurement of the LNA bias current is used to guide the calibration. The tunable element proposed in [17] is a tunable transmission line stub that can be shorted at discrete lengths to change the loading conditions of a 28 GHz PA. An iterative test-and-tune calibration loop is employed to search for the optimum position of the tuning knobs. Embedded instruments for current, power, and temperature measurements are used to monitor the performance of the PA in the calibration process.

The concept of digitally controlled transmission lines is also exploited in [18], [19]. In [18], authors demonstrate a 60 GHz amplifier where tunable transmission lines are employed to mitigate the shift of the s-parameters due to process variations. The proposed tunable transmission line is built as a differential coplanar transmission line with an array of floating metal finger pairs underneath. These metal fingers can be shorted to a fixed voltage, resulting in an effective change of the dielectric permittivity.

The work in [19] demonstrates a calibration procedure for 60 GHz LNA that is able to significantly reduce the power consumption and NF dispersion due to process variations. The proposed calibration loop is based on monitoring the DC voltage at an internal node of the LNA and the device temperature. Two tunable elements are provided. The first one is a DAC that tunes the bias current of the LNA, while the second one is a digitally controlled transmission line that allows tuning the loading impedance of the LNA.

A tunable linearization block based on a feedback bias/capacitive scheme is presented in [20]. Three DC bias voltages are used to tune the operation of the linearization block and reduce the impact of process variations in a 60 GHz PA. The proposed calibration algorithm requires sweeping the input power of the PA and monitoring the output power.

The tunable elements and measurement instruments that have been presented in the literature enable calibration capabilities at the cost of increasing the design complexity, especially as the operating frequency increases. Moreover, many of the proposed tuning knobs and embedded instruments are dedicated solutions tailored to a given circuit family or even to a particular circuit architecture. Authors outlined in [4] a machine learning-based calibration solution aimed at simplifying this design complexity. The proposed solution was based on the use of a novel variable decoupling capacitor as a tuning knob. Electrical simulation results on a preliminary case study validated the technique.

In this paper, we extend our previous work by demonstrating the feasibility and performance of this technique with the design and experimental characterization of an integrated proof-of-concept prototype featuring the proposed calibration technique. Compared to the state-of-the-art, the proposed prototype combines the optimized nonintrusive performance monitoring developed by the authors in [22] with the use of low design complexity and generic tuning knobs that do not require modification of the circuit power supply. In this regard, this paper presents a 69 GHz PA with embedded one-shot calibration and non-intrusive performance monitoring. The demonstrator has been integrated in STMicroelectronics 55 nm CMOS technology. Experimental results on a set of 39 fabricated samples demonstrate the feasibility and performance of the proposed calibration in two different application scenarios. Firstly, the proposed calibration technique is employed in the context of yield enhancement to recover fabricated samples that, due to

excessive process variations, do not comply with the nominal design targets. Secondly, we further extend the application of the proposed one-shot calibration to demonstrate aggressive performance tuning to address different performance trade-offs.

III. Theoretical Basis

A. One-Shot Statistical Calibration

Statistical calibration, also known as machine learning-based calibration in the literature, is a calibration technique that employs a machine learning regression algorithm to guide the tuning process. Initial works in this line follow the standard calibration scheme in Fig. 1 but instead of a direct measurement of the circuit performance, they employ regression algorithms to predict the circuit performance in each iteration of the calibration algorithm from a set of indirect measurements [16]. More advanced statistical calibration techniques, on the other hand, employ machine learning algorithms to predict, directly, the best combination of tuning knobs from a set of circuit measurements, to comply with a set of predefined design goals. The need for multiple iterations in a test-and-tune loop is then avoided. These calibration techniques are usually known as one-shot statistical calibration techniques. In this manuscript, we will focus on one-shot techniques.

Let us consider that the circuit under calibration has a set of n performances $\mathbf{P} = [P_1, P_2, \ldots, P_n]$ and k tuning knobs $\mathbf{T} = [T_1, T_2, \ldots, T_k]$. In a one-shot statistical calibration, the objective is to find a set of simple measurements (i.e., signatures) $\mathbf{S} = [S_1, S_2, \ldots, S_l]$ such that we can build a regression function f as

$$f : [T_1, \ldots, T_k, S_1, \ldots, S_l] \rightarrow [P_1, P_2, \ldots, P_n]\,. \qquad (1)$$

Assuming that such a regression function f can be determined, the calibration procedure for each fabricated circuit sample would be reduced to measuring the signature vector $[S_1, \ldots, S_l]$ for this particular sample and then employing function f for exploring the space of tuning knob positions $[T_1, \ldots, T_k]$ to tune the circuit performances $[P_1, \ldots, P_n]$ according to the design specifications.

The regression function f can be obtained using a supervised machine learning regression algorithm. This procedure is divided into two stages: in the first stage –the training stage– for a small population of fabricated circuits (i.e., the training set) both the performances and the signatures are extracted under different combinations of tuning knobs. The resulting data set (i.e., the training data) is then employed to train a machine learning regression model that maps the circuit performance to the signature measurements and the tuning knob states. Then in a second stage –the calibration stage– for each fabricated circuit in the production line only the set of signatures is measured (under nominal tuning knob positions) and the machine learning model previously obtained is used for determining the best combination of tuning knobs to comply with the design specifications. The process has the advantage of avoiding iterative calibration loops since the regression function allows finding the optimum calibration point in one shot. The disadvantage with respect to the iterative calibration is the need of the training phase, which requires the measurement of a number of circuits to obtain the training data set. It has to be noted, however, that this training is performed only once on a limited subset of circuits and is then applied directly to the full production. The proposed technique is then particularly suitable for large circuit populations, or for high-precision calibration that would require a large number of iterations. Further discussion on the generation of appropriate training data and the trade-off between the number of training samples and regression accuracy will be offered in later sections.

B. Nonintrusive Process Variation Monitoring

One of the key points for enabling one-shot statistical calibration methods is to propose a suitable set of signatures $[S_1, S_2, \ldots, S_l]$ such that a meaningful regression function f can be built. In other words, we need to find a set of indirect measurements that are strongly correlated to the circuit performance, in such a way that a machine learning algorithm can then extract a reliable mapping function f that accurately reflects the main degradation mechanisms affecting the circuit performance.

In this paper, to guide the calibration algorithm, we adapt the nonintrusive test methodology proposed by the authors in [22]. In this regard, we propose to integrate a set of nonintrusive process monitors together with the circuit under calibration. These process monitors are stand-alone circuits, not connected to the circuit under calibration, that are designed to output DC or low-frequency signatures sensitive to the variations of a selected set of physical parameters in the fabricated silicon. By targeting the physical parameters critical for the performance of the circuit, it is possible, as demonstrated in [22], to train a machine learning model to predict the performance of the fabricated circuit from the process signatures provided by the monitors. In this work, and given that the process signatures are strongly correlated to the circuit performances, we propose to employ this nonintrusive on-chip monitoring strategy to guide the calibration algorithm and provide the signatures to train the regression function in (1).

IV. Design of a mm-Wave Power Amplifier With Nonintrusive One-Shot Calibration

A. Overall System Architecture

The main goal of this paper is to experimentally demonstrate a practical mm-wave PA with embedded calibration based on the concepts of one-shot statistical calibration and nonintrusive process monitoring discussed in the previous section. Conceptually, the system block diagram is similar to the one in Fig. 1, with the particularity that measurements come from process monitors not connected to the circuit under calibration. These monitor circuits generate a set of DC and low-frequency signatures that are strongly correlated with the PA performance. These signatures are read out by a machine learning algorithm that predicts the best positions of the PA tuning knobs to optimize the PA performance according to the calibration targets. The following subsections detail the design

TABLE I
POWER AMPLIFIER DESIGN TARGET

DC current, I_{DC}	< 30 mA
Power supply, V_{DD}	1.2 V
Gain (S_{21})	$\in [9,\ 10]$ dB @ 69 GHz
Power Added Efficiency, *PAE*	$> 12\%$
Output 1dB-Compression Point, CP_{1dB}	> 6 dBm
Saturation output power, P_{sat}	$\in [9.5,\ 10.5]$ dBm
S_{11}	< -10 dB
S_{12}	< -15 dB

of the proposed system, especially focusing on the proposed tuning knobs, the set of on-chip process monitors, and the practical implementation of the calibration algorithm.

B. Power Amplifier Circuit Core

The core of the PA is a 2-stage class A 69 GHz power amplifier designed in STMicroelectronics 55 nm CMOS technology. The choice of a 2-stage structure provides a compelling validation for the proposed calibration strategy since the interactions between the different circuit elements, including both active devices and full-custom passive structures, make calibration a complex task. In this regard, it is worth noticing that this work does not target the design of a state-of-the-art PA for any particular application, but to offer a compelling demonstration of the proposed calibration technique in a challenging case study.

The PA is composed of two stages of common source NMOS transistors in class A operation. The matching networks use a structure based on microstrip transmission line stubs. Fig. 2 shows the transistor-level schematic. The output network has been designed to maximize the output compression point. Table I summarizes the design target performance for the PA.

As is shown in Fig. 2, the gate bias voltage of the transistors and the decoupling cells have been made programmable to enable tuning capabilities. Concerning the decoupling capacitor banks, they have been modified by embedding varactors to provide variable termination loads for the stubs in the matching networks. From a designer's point of view, they act as both a standard decoupling cell and an impedance tuner. The functionality of these structures is further explored in the next subsection.

C. Design of the Tuning Knobs

Together with the PA, we have implemented a total of six tunable elements for calibration purposes: two DC gate bias voltages, labeled V_{B1} and V_{B2} in Fig. 2, and four variable decoupling cells, labeled C_{V1} to C_{V4} in Fig. 2. These six tuning knobs are controlled by DC voltages provided by the calibration algorithm, as conceptually depicted in Fig. 1. By programming the DC voltage applied to the tuning knobs, it is possible to modify the DC power consumption of the circuit and the impedance at different internal nodes. Thus, the DC gate bias voltages V_{B1} and V_{B2} offer a direct control on the current consumption of the two stages of the amplifier, but they also have an impact on the gate and drain impedances of the transistors since MOS transistor parasitic capacitances

TABLE II
SIMULATED PA PERFORMANCE WITH AND WITHOUT VARIABLE DECOUPLING CELLS

	PA without tuning knobs	**PA with tuning knobs**
I_{DC}	29 mA	29.2 mA
S_{21}@ 69 GHz	9.3 dB	9.2 dB
PAE	12.9%	12.7 %
CP_{1dB}	7.1 dBm	7.1 dBm
P_{sat}	10.3 dBm	10.4 dBm
S_{11}@ 69 GHz	< -10 dB	< -10 dB
S_{12}@ 69 GHz	< -15 dB	< -15 dB
k stability factor	> 1.9	> 1.9

are bias-dependent. The variable decoupling cells are used as termination loads for the stubs in the matching networks. Their impedance value is low enough to work as a decoupling cell at 69 GHz, and since their impedance can be programmed, they provide the ability to modify the impedance matching between the different elements of the PA. The proposed tuning solutions have the advantage of avoiding a complex co-design of the tuning knobs within the PA architecture.

Concerning the variable decoupling cells, their working principle can be detailed as follows. Fundamentally, a decoupling cell is employed to guarantee a constant DC voltage in a given node. In essence, a decoupling cell is simply a capacitor whose value is high enough to provide an AC short circuit at the operating frequency, which results in a constant DC voltage in a given node. For our target calibration application, this capacitor has been replaced with a variable capacitor, implemented with a varactor and a MOM capacitor in series. Fig. 3 shows an electrical schematic of the proposed variable decoupling cell. A total of 20 unit cells (varactor plus MOM capacitor) are connected in parallel to achieve a low enough impedance value at the working frequency for a total capacitance of 1.25 pF, i.e., $0.5 - j1.7\,\Omega$ at the PA operation frequency and a nominal control voltage of 1 V. Depending on the voltage applied to the control node, the decoupling cell provides an imaginary impedance value that can be programmed between $-2.3\,\Omega$ and $-1.1\,\Omega$. Fig. 4 represents the variation of the proposed programmable decoupling cell when the control voltage varies from -1 V to 2.5 V. The quality factor varies between 2 and 4.8. Although narrow, it will be shown that this variation range is sufficient for the purpose of this work. For comparison, notice that the impedance of a standard decoupling cell built with six 0.2 pF MOM capacitors in parallel displays a similar impedance ($0.5 - j1.8\,\Omega$), as represented in Fig. 4, and quality factor $Q = 4.2$. According to electrical simulations, the quality factor of the decoupling cell has a negligible impact on the performance of the amplifier, therefore it is not a critical design element. This was verified by simulating the PA with and without the variable decoupling cell. Table II shows a direct comparison of the PA specifications obtained by electrical simulations for the typical corner of the technology, with and without the variable decoupling cells. No significant deviation was observed for any of the PA performances in Table II between the two versions of the PA and the PA remains unconditionally stable.

To illustrate the functionality of the proposed tuning knobs

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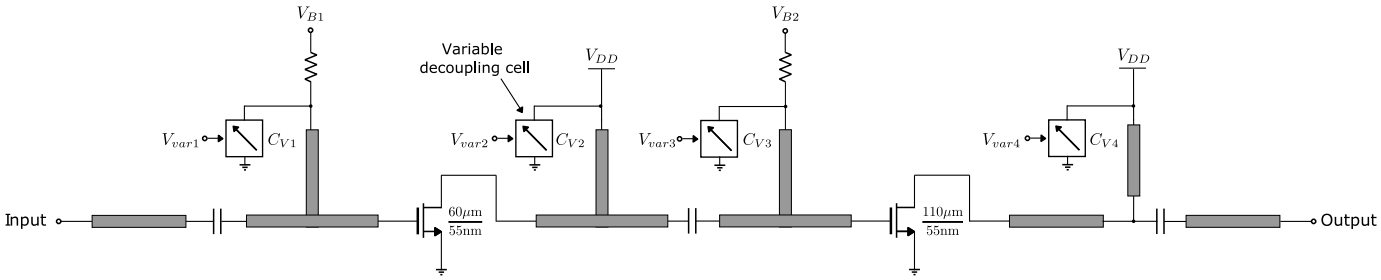

Fig. 2. Transistor-level schematic view of the 2-stage PA and tuning knobs.

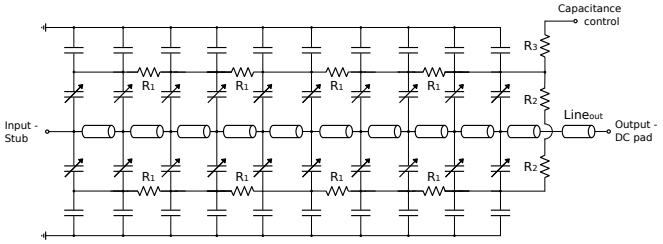

Fig. 3. Electrical schematic view of the variable decoupling cell proposed as tuning knob.

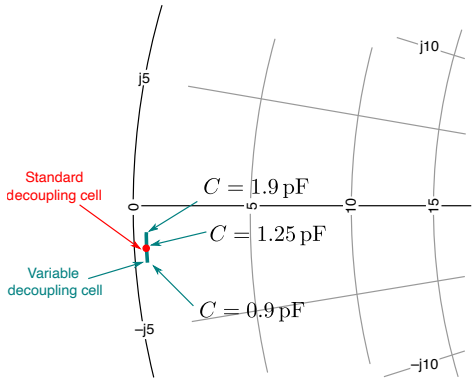

Fig. 4. Impedance variation range of the proposed variable decoupling cell at 69 GHz for a variation of the control voltage from -1 V to 2.5 V.

and how they may be used to compensate for process variations, let us examine the electrical simulation results from a simplified example in Fig. 5. Let us consider an output matching network designed to match the optimal impedance Z_{opt} to be presented to the drain of a transistor to maximize the PAE for a given input power. In the nominal (i.e., ideal) case, the network may be able to present a matched impedance $Z_{network} = Z_{opt}$. However, the actual values of Z_{opt} and $Z_{network}$ after fabrication will differ from the nominal due to process variations, which results in $Z_{network} \neq Z_{opt}$. The proposed tunable elements, that is, in this simplified case, the transistor gate bias voltage and the output network decoupling cell impedance may be used to recover the ideal matching. Indeed, by varying the gate bias voltage, the required Z_{opt} is modified, and by varying the decoupling cell impedance the actual $Z_{network}$ may be also modified resulting in an approximate matching, $Z_{network} \approx Z_{opt}$, after calibration. For illustration purposes, Fig. 5 presents a Smith chart on which we have represented impedances Z_{opt} and $Z_{network}$ obtained by electrical simulations. The required Z_{opt} for different process corners are represented by red dots. For a PA in the typical corner, the Z_{opt} excursion obtained by changing the transistor gate bias is plotted in a pink dashed line and the $Z_{network}$ excursion obtained by changing the decoupling cell bias is plotted in a blue line. It is clear to see that the complete corner variation area is reachable by varying these tuning knobs.

Moreover, it should be noticed that varying the gate bias voltages also has a direct effect on other key performance parameters, such as the linearity or the power consumption of the PA. To give a deeper insight into the feasible tuning space when varying the complete set of 6 tuning knobs in the PA, Table III shows the lower and upper reachable boundaries for each PA specification obtained by electrical simulation in the typical corner. The target PA specifications are also listed in Table III for reference. The considered variation ranges for the tuning knobs were of $[0.6, 1]$ V for the bias voltages, V_{B1} and V_{B2}, and of $[-1, 2.5]$ V for the variable decoupling capacitor bias voltages, V_{var1} to V_{var4}. It is clear to see that the proposed tuning knobs offer a very wide variation range for s-parameters, going even beyond the functional limits of the amplification function, whereas there is also a significant tuning range for linearity specifications. Moreover, the amplifier remains stable in all the considered tuning range, and the amplifier's bandwidth is not significantly affected by the tuning knobs either. It is worth noticing that these results should be interpreted in the context of the multidimensional interactions between tuning knobs and specifications. That implies, for instance, that the upper (or lower) limit for each specification in Table III corresponds to different combinations of tuning knobs. By relying on a multidimensional regression model for performing the calibration, we are able to perform a global optimization of the circuit performance that naturally takes into account these complex multi-parameter interactions, as will be demonstrated in later sections.

Concerning the extension of these techniques to other PA architectures beyond our case study, the described tuning knobs are generic and simple enough to be readily incorporated into other architectures with minimum design modifications. However, it should be noticed that more complex amplifier structures, such as power combining PAs, distributed amplifiers, Doherty amplifiers, etc., may require additional tuning knobs if the expected performance variation range exceeds the correction capabilities of the proposed tuning

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TABLE III
BOUNDARIES OF THE REACHABLE TUNING SPACE FOR EACH SPECIFICATION OF A PA IN THE TYPICAL CORNER

	Lower boundary	Upper boundary	Design target
I_{DC}	9 mA	48 mA	< 30 mA
S_{21}@ 69 GHz	0.6 dB	12 dB	$\in [9,\ 10]$ dB
PAE	0.1 %	17 %	$> 12\%$
CP_{1dB}	4.5 dBm	10.2 dBm	> 6 dBm
P_{sat}	7.6 dBm	10.8 dBm	$\in [9.5,\ 10.5]$ dBm
S_{11}@ 69 GHz	-27.6 dB	-4.8 dB	< -10 dB
S_{12}@ 69 GHz	-25.3 dB	-16.6 dB	< -15 dB

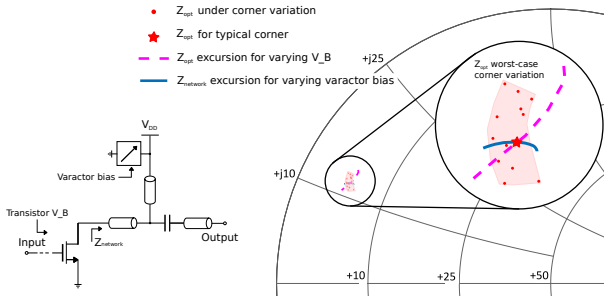

Fig. 5. Working principle of the variable decoupling cell as a tuning knob, illustrated with electrical simulation results.

knobs or if different calibrated performances are targeted (for instance, calibrating the bandwidth in a wideband amplifier). Considering each particular case study is beyond the scope of this paper. However, it should be noticed that the choice of a machine learning-based calibration strategy greatly simplifies the addition of tuning knobs. Traditional iterative calibration strategies usually rely on orthogonal tuning knobs (i.e., each tuning knob affects, independently, a performance or a group of performances) to reduce the number of search iterations. In practice, this is a strict requirement that makes the design of tuning knobs (or the addition of new ones) a challenging task. In a statistical calibration, the multidimensional correlations between tuning knobs and performances are naturally managed by the learning algorithm, effectively removing this requirement for the design of the tuning knobs. In this regard, any other tuning knob presented in the literature can be considered as a potential candidate to enhance the set of tuning knobs, and the effectiveness of the resulting tuning knob set can be evaluated as a function of the accuracy of the resulting calibration function f in (1).

D. Design of the Nonintrusive Process Monitors

As explained in previous sections, the calibration algorithm is controlled by the readings of several on-chip process monitor circuits that have been integrated together with the PA. These process monitor circuits have to be specially designed to be sensitive to the main performance degradation mechanisms of the PA. Authors presented in [22] a systematic methodology for the design of these process monitors in the context of mm-wave circuit testing. The design methodology for the proposed calibration application is a natural extension of the one presented in [22].

In essence, we need to design process monitors that provide a set of signatures, i.e., simple measurements, that are

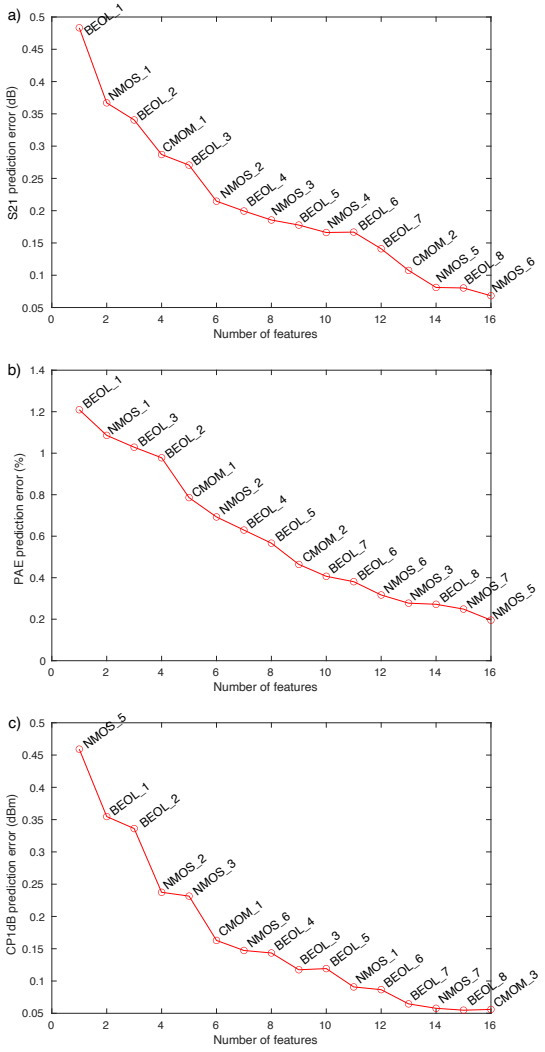

Fig. 6. Learning curves: prediction error of the amplifier's a) S_{21}, b) PAE, and c) *CP1dB* as a function of the number of process parameters selected as input features. Process parameters, labeled for each data point, are added from more relevant to less relevant to the prediction of the target performance.

strongly correlated to the circuit performance degradation due to process variations. The proposed design methodology is divided into two steps. The first step is aimed at identifying the main root causes of performance degradation among the different physical parameters affected by process variations during production. Then in a second step, we target the design of simple circuit structures that are sensitive to the set of identified physical parameters.

Following the design methodology in [22], to identify the root causes of performance degradation in an electrical simulation environment, we can run a search algorithm in the space of process variation parameters defined in the Monte Carlo and corner models in the Process Design Kit (PDK) of the selected technology. This algorithm, based on feature selection techniques, is designed to identify the subset of process variation parameters that are relevant for explaining the variation observed in the circuit performance under process variations. Detailing the functionality of this search algorithm is out of the scope of this paper. The interested readers are

referred to [22] for a thorough explanation.

If we consider the proposed two-stage PA in STMicroelectronics 55 nm CMOS technology, the PDK of the selected technology contains more than 500 independent process variation parameters. A search in the space of process parameters based on 1000 instances of the PA generated using Monte Carlo simulation, reveals that the main performance figures of the PA (i.e., s-parameters, 1-dB compression point, saturation power, power added efficiency, and current consumption) are determined (to an accuracy about 1%) by a subset of only 16 technological parameters. For illustration purposes, Fig. 6 (a), (b), and (c) show three learning curves for the amplifier S_{21}, *PAE* and CP_{1dB}, respectively. These learning curves represent the evolution of the Root-Mean-Square (RMS) prediction error of regression models for these performances, as a function of the number of process parameters considered as input features for such regression models. Process parameters are added to the models according to their relevance, as determined by the proposed search in the process parameter space. Simple perceptron models with 15 neurons in the hidden layer are considered for this validation. The RMS prediction error is computed on 200 independent validation samples generated using Monte Carlo simulation. Due to confidentiality reasons, we cannot disclose the actual names of these process parameters in the PDK. Instead, we have labeled the identified parameters as *NMOS_x*, *CMOM_x*, and *BEOL_x*, indicating that they correspond to variations of the NMOS transistors, MOM capacitors, and features of the technology Back-End-Of-Line (BEOL), respectively. As can be seen, the set of identified parameters reflects a trade-off between inter-stage and load adaptation, electrical losses, and the transistors operation points, as could be expected by an electrical analysis of the circuit in Fig. 2. Moreover, it is interesting to observe that the most relevant process parameters for the prediction of large signal and small signal performances differ, as can be clearly observed in Fig. 6.

Once the set of relevant parameters is identified, we designed a set of circuit structures that generate simple signatures strongly correlated with the identified parameters. Table IV shows the designed nonintrusive process monitor circuits, the signatures generated from each process monitor, and to which process parameters they are correlated. We have designed five process monitors, a high-impedance transmission line, a low-impedance transmission line, a MOM capacitor, a MOS junction capacitance monitor, and a MOS transistor. We have defined nine low-frequency or DC signatures. Since these signatures are designed to be strongly correlated to the same process parameters correlated to the PA performances (see Fig. 6), it follows that both the proposed signatures and the PA performances should be also strongly correlated. In this work, as a proof-of-concept, we target the measurement of these signatures using external test equipment. It has to be noted, however, that the test equipment requirements for signature extraction are greatly reduced compared to the resources needed for a functional test of the PA under calibration.

It is worth noticing that the proposed methodology is generic and can then be directly applied to other PA architectures. Needless to say, different PA topologies and different target specifications not studied in this work (for instance the amplifier's bandwidth in wideband designs) may lead to the design of a different set of process monitor circuits and signatures depending on the identified relevant process parameters for each case.

E. Machine Learning-Based Calibration Algorithm

As has been said above, the described calibration algorithm has the goal of predicting the best position of the tuning knobs for each fabricated PA sample –in our case the values of the DC tuning voltages V_{B1}, V_{B2}, V_{var1}, V_{var2}, V_{var3}, and V_{var4}– to comply with a given design target, as a function of the readings of the process monitor circuits embedded in each particular sample. The key element for this calibration technique is the regression function f that maps the output of the process monitors and the positions of the tuning knobs to the performance of the PA.

In this work we train a machine learning regression model, namely a perceptron neural network with one hidden layer composed of 15 neurons, to build this regression function. Training is performed in a classical supervised-learning fashion [24], as conceptually depicted in the flow chart in Fig. 7. Firstly, a number of PA samples, N_T, are set apart as a training set to generate the data for training the neural network. Then, in a second stage, the trained regression model is deployed for the rest of the fabricated samples in the production line. To generate the data set required for training the neural network, it is required to measure the set of process monitor signatures and the PA performance under N_C combinations of tuning knob positions for each of the N_T PA samples in the training set. The efficient generation of an appropriate training set is discussed in detail in the following section.

Once the regression function f is available, and given a set of target specifications, the optimum position of the tuning knobs for each fabricated sample can be determined by measuring the process signatures for that particular sample $[S_1, \ldots, S_9]$ and then minimizing the cost function F,

$$\begin{aligned} &F(V_{B1}, V_{B2}, V_{var1}, \ldots, V_{var4}) = \\ &\|f(V_{B1}, \ldots, V_{var4},\, S_1, \ldots, S_9) - [P_1^t, \ldots, P_n^t]\|, \end{aligned} \tag{2}$$

where $[P_1^t, \ldots, P_n^t]$ represents the target design performance and $\|\cdot\|$ is the Euclidean distance operator, under the constraints,

$$\begin{aligned} &P_i \in [P_i^L,\, P_i^U], \forall i \\ &V_j \in [V_j^L,\, V_j^U], \forall j, \end{aligned} \tag{3}$$

where P_i^L and P_i^U represent the lower and upper bounds of performance P_i defined by the target specifications, respectively, and V_j^L and V_j^U are the lower and upper limits of the variation range for each of the tuning voltages V_j, respectively. Hence, the value of vector $[V_{B1}, V_{B2}, V_{var1}, \ldots, V_{var4}]$ that minimizes function F and complies with the defined constraints would yield the closest performance to the design targets that is attainable by a given PA sample. The proposed cost function is then biased to center the specifications around a target. It is worth noticing that different definitions are possible for the cost function if other design requirements

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TABLE IV
DEVELOPED NONINTRUSIVE PROCESS MONITORS AND ASSOCIATED SIGNATURES FOR GUIDING THE PA CALIBRATION ALGORITHM

Process control monitor schematic	Signature description	Correlated process parameters
High-impedance microstrip line Input — Output	• S_1: Imag part of S_{11} @ 1 GHz • S_2: Imag part of S_{21} @ 1 GHz • S_3: Resistance	• *BEOL_1*, *BEOL_2*, *BEOL_5*, *BEOL_3* • *BEOL_1*, *BEOL_2*, *BEOL_8*, *BEOL_7* • *BEOL_2*
Low-impedance microstrip line Input — Output	• S_4: Imag part of S_{11} @ 1 GHz	• *BEOL_5*, *BEOL_4*, *BEOL_7*, *BEOL_6*
MOM capacitor Input — Output	• S_5: Real part of Y_{11} @ 1 GHz • S_6: Imag part of S_{21} @ 1 GHz	• *CMOM_1*, *CMOM_3* • *CMOM_2*, *CMOM_3*
Junction capacitance sensor Input	• S_7: Imag part of S_{11} @ 1 GHz	• *NMOS_4*, *NMOS_7*, *NMOS_2*, *NMOS_6*
NMOS transistor 0.9V, 1.2V Input, Output	• S_8: Gate resistance = $\mathrm{Re}(Y_{11})/\mathrm{Im}(Y_{11})^2$ • S_9: Bias current	• *NMOS_1*, *NMOS_2*, *NMOS_5*, *NMOS_3* • *NMOS_5*, *NMOS_7*

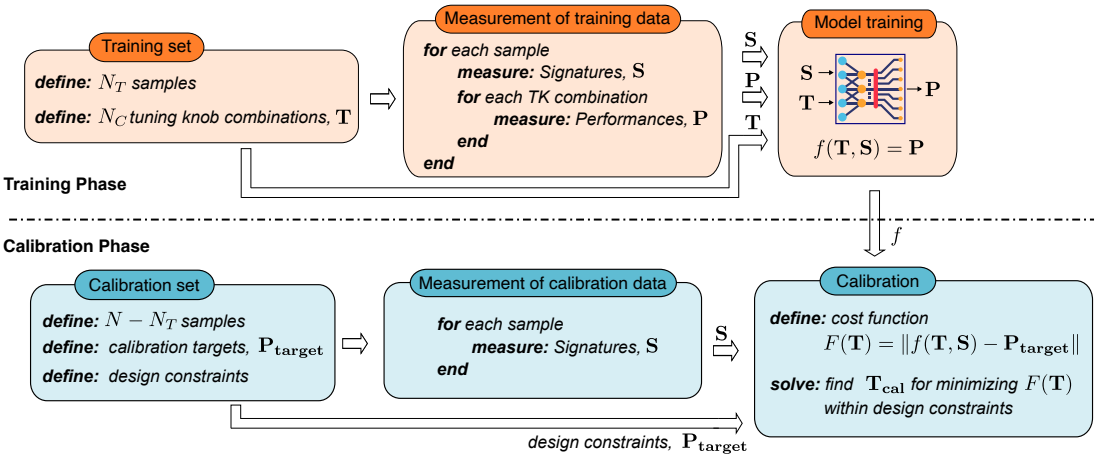

Fig. 7. Conceptual flow chart for the proposed machine learning-based one-shot calibration.

are targeted. Indeed, by defining a different cost function or modifying the constraints, it may be possible to recenter the circuit performance, within its tunability limits, to address different application scenarios and/or performance trade-offs. Once the process monitor readings are measured and the target specifications are defined, this recentering application does not need the retraining of the machine learning regression function f, which can be readily reused to predict, in one shot, the best combination of tuning knobs for the newly defined application scenario.

In this work, for the sake of proof-of-concept validation, both the perceptron neural network and the cost function minimization algorithm have been implemented externally using Matlab.

F. Generation of Training Data

As is the case with any machine learning-based technique, defining an appropriate training set is crucial for obtaining an accurate predictive model for our calibration methodology. Simply put, a machine learning model is as good as its training data. Thus, a first concern in the generation of the training data should be the accuracy of the required measurements. Both the signatures and the PA performances are measured for all the training samples. The accuracy of these measurements represents a practical limit for the accuracy of the machine learning predictions, and hence, for the accuracy of the calibration. Nevertheless, this is also the case for traditional iterative calibration where only functional measurements are performed.

A second concern is the complexity of the considered machine learning algorithm. Complex models with a large

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number of parameters, such as state-of-the-art deep learning algorithms, require a large number of training samples. This is the main reason that in this work we consider a simple perceptron model, which offers a good trade-off between model complexity and accuracy relaxing this way the need for a large training set.

A third concern is the variety of the training data. Training a machine learning model requires a significant training data set to accurately capture the correlations between the input features and the output targets. As depicted in Fig. 7, in our calibration problem, two key parameters define the training set: the number of circuit samples set apart for training, N_T, and the number of different tuning knob positions considered for each sample, N_C. Increasing the product $N_T \times N_C$ enhances the training set and improves the accuracy of the resulting model, but at the same time increases the cost of the calibration, since the number of functional measurements for training also increases. A trade-off arises between the accuracy of a machine learning-based calibration and its cost. The cost of the proposed nonintrusive machine learning-based calibration can be modeled as,

$$C_{ML} = C_{train} + C_{cal} = N_T(N_C D + I) + (N - N_T)I, \quad (4)$$

where C_{train} and C_{cal} are the costs associated to the training and calibration phases, respectively, N is the total number of fabricated samples in the production, D is the cost of the direct performance measurements, and I is the cost of measuring the indirect signatures. For reference, the cost of a standard iterative calibration can be modeled as,

$$C_{iter} = N N_i D \leqslant N N_C D \quad (5)$$

where N_i is the number of iterations required for calibration. By comparing (4) and (5) and taking into account that the indirect signatures are designed to be cheaper than standard direct measurements, it is easy to see that a machine learning-based calibration becomes advantageous compared to traditional calibration for a large production of circuits ($N >>$), if the product $N_T \times N_C$ can be reasonably contained. This trade-off can be further analyzed by considering the learning curves representing the error in the prediction of the PA performances (i.e., the accuracy of the calibration) as a function of the number of training samples and the number of considered tuning knob positions.

In order to illustrate this analysis, Fig. 8 (a) and (b) show the evolution of the prediction error of the amplifier's PAE as a function of the number of training samples (for the nominal positions of the tuning knobs) and the number of tuning knobs combinations (for a fixed number of training samples $N_T = 40$, blue circle markers), respectively. These learning curves have been obtained based on Monte Carlo simulations by computing the RMS prediction error in an independent test set. Again, a perceptron model with 15 neurons in the hidden layer is employed in the analysis.

Concerning N_T, Fig. 8 (a) shows a saturation of the prediction error around $N_T \simeq 100$ samples. A similar result can be obtained for the rest of the amplifier's performances. It is worth pointing out that these results are highly dependent on the particular case study. Other PA architectures may require a different number of training samples. In any case, the proposed analysis based on learning curves is completely generic and readily applicable to other case studies.

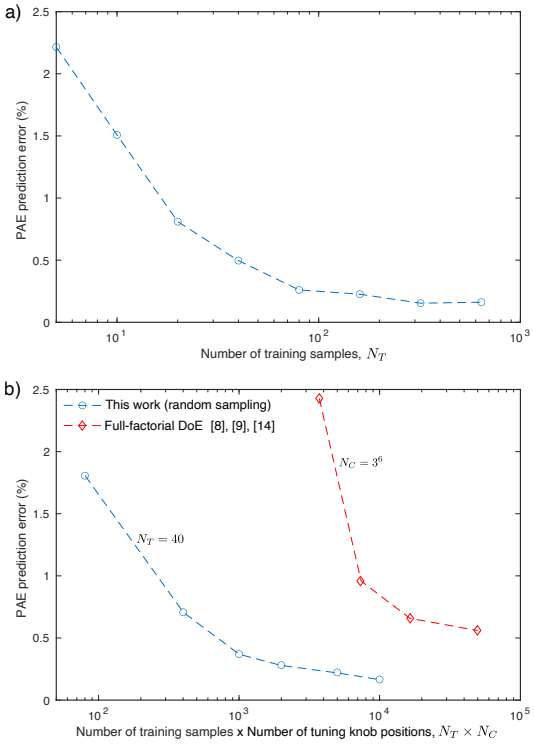

Fig. 8. Learning curves: Evolution of the PAE prediction error as a function of a) the number of training samples; and b) the number of considered tuning knob combinations for the proposed random sampling method (blue circle markers), compared to the traditional full-factorial approach (red diamond markers).

Analyzing the influence of the number of tuning knob positions employed for training requires further considerations. Previous works on machine learning-based calibration propose a full-factorial Design-of-Experiment (DoE) approach [8], [9], [14], inherited from traditional iterative calibration strategies. That is, if the circuit under calibration has k tuning knobs, p fixed positions evenly distributed are considered for each tuning knob (for instance, a usual choice is to consider minimum, typical, and maximum values), resulting in $N_C = p^k$ possible combinations. This approach has two key problems that make it not suitable for machine learning-based calibration. The first issue is that the number of tuning knob combinations N_C explodes as the number of tuning knobs increases. If we consider the cost model in (4), this means that the machine learning-based calibration would be less appealing as the complexity of the circuit under calibration increases. The second issue is related to the nature of learning machines. A learning algorithm requires variety of data to learn. By repeating the same tuning knob positions for each sample, the learning process is actually hindered.

In this work, we present a solution to these issues, adapted from our work in [23]. The data generation strategy in [23] relies on random sampling of the tuning knob positions to generate varied data for training. However, it assumes that

$N_T = N_C$ so the variety in training data comes at the cost of increasing the number of required training samples. In this work, we propose instead to measure a set of N_C random positions of the tuning knobs for each of the N_T samples in the training set. Values are drawn from a uniform distribution between the minimum and maximum values for each tuning knob. In this way, variety is ensured to improve the training without the need to increase the number of training samples. The value of N_C, now decoupled from the value of N_T, can be determined by its associated learning curve. To exemplify this technique, Fig. 8 (b) shows the evolution of the prediction error of the amplifier's PAE as a function of N_C for a fixed value of $N_T = 40$ (blue circle markers). For comparison, Fig. 8 (b) also shows the learning curve for a standard full-factorial strategy, as proposed in [8], [9], [14], for three positions of the tuning knobs (min., typ. and max.), i.e., $N_C = 3^6 = 729$ possible combinations, as a function of the number of training samples N_T (red diamond markers). The x-axis of the figure represents the product $N_T \times N_C$ for a direct comparison. In the view of the cost model (4), the advantage of the proposed random sampling for training set generation becomes clear. A better accuracy is achieved with the proposed random sampling while significantly reducing the amount of required training data. To put these results in perspective, we can also compare them with published iterative calibration methods. For instance, [17] proposes, for each sample under calibration, an exhaustive search in a space of $N_C = 262\,144$ tuning knob combinations for maximizing the output power of a PA. Similarly, the work in [18] relies on a full search in a space of $N_C = 65\,536$ possible combinations. Taking into account the cost function (5), it is easy to see how the cost of iterative calibration may become prohibitive for large values of N.

V. Experimental Results

A. Characterization of the Proposed PA for Nominal Positions of the Tuning Knobs

The proposed 2-stage 69 GHz PA with embedded calibration has been fabricated in the selected 55 nm CMOS technology. Fig. 9 shows a microphotograph of the complete system including the 2-stage PA with tuning elements and the set of process monitor circuits, together with a floorplan detailing the positions of the main circuit elements (in the microphotograph there are three additional structures not related to this project). The system occupies an area of $690\,\mu\text{m} \times 1090\,\mu\text{m}$ and, as it can be observed, the process monitor circuits have been placed in the free space left between the passive components of the PA. It should be noted that the area overhead of the process monitors is dominated by the area of the dedicated test pads for each process monitor. In an actual application, the test pads would be multiplexed, further reducing this way the effective area overhead. In any case, to put these areas in perspective, it should be noticed that the area of published mm-wave transceivers is, on average, above $4\,\text{mm}^2$ per Tx/Rx pair, and multiple Tx/Rx pairs are implemented in a state-of-the-art beamforming transceiver [25]–[27]. The total area of the on-chip process monitors, including pads, is $0.34\,\text{mm}^2$, which is negligible compared to the area of a complete mm-wave transceiver.

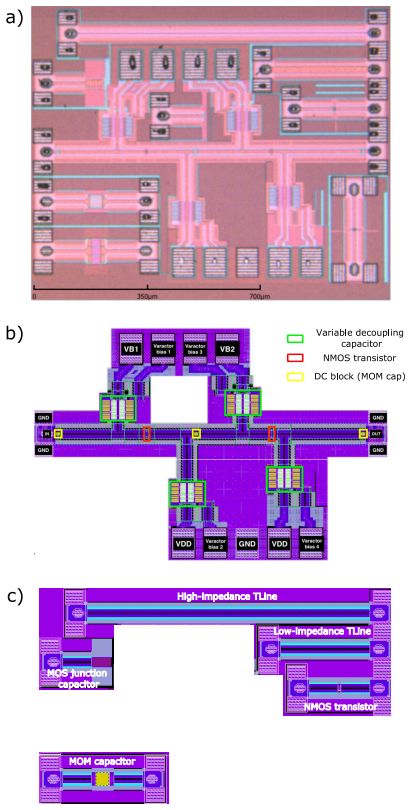

Fig. 9. a) Microphotograph of PA with embedded calibration; b) Floorplan of PA and tuning knobs; c) Floorplan of nonintrusive process monitor circuits.

We have received a set of 39 fabricated PAs that contain samples from both the center and the borders of the wafer to better observe the effects of process variations. Firstly, to verify the functionality of the fabricated PAs, the 39 samples have been characterized in the laboratory under nominal conditions. The power supply has been set to $V_{DD} = 1.2\,\text{V}$ and the tuning knobs have been set to $V_{B1} = V_{B2} = 0.9\,\text{V}$, $V_{var1} = V_{var2} = V_{var3} = V_{var4} = 1\,\text{V}$. These tuning knob values correspond to a centered performance under typical corner conditions. Table V shows the measured max. min. and average performance for the set of fabricated PAs under nominal biasing conditions. Fig. 10 and 11 show the measured s-parameters and the compression characteristic, respectively, for a representative uncalibrated sample of the PA. Measurements have been carried out using an Anritsu ME7838D VNA, Cascade S300 semi-automatic probe station, and 145 GHz Infinity Probes from Cascade. Large signal measurements employ a Spacek Labs PA to drive the PA under test.

In addition, Table V shows the fabrication yield taking into account the target specifications. It has to be noted that yield can only be properly computed at industrial level in high-volume production. In our academic case study, we are limited to a few fabricated samples. In this work, we denote as yield the proportion of circuits within the target specifications over the total fabricated samples. Regarding the specification test limits, they are significantly more stringent than the 3σ variation range obtained by Monte Carlo simulation. The

TABLE V
POWER AMPLIFIER MEASURED PERFORMANCE SUMMARY FOR 39 FABRICATED SAMPLES BEFORE CALIBRATION

	Design target	Min.	Max.	Average	Yield
S_{21}@69 GHz	$\in [9,\ 10]$ dB	8.2 dB	11.9 dB	9.5 dB	51% (20 out of 39)
PAE	$> 12\%$	4.4%	15.5%	9.7%	31% (12 out of 39)
CP_{1dB}	> 6 dBm	4.6 dBm	8.8 dBm	6.9 dBm	77% (30 out of 39)
P_{sat}	$\in [9.5,\ 10.5]$ dBm	6.7 dBm	10.4 dBm	9.7 dBm	74% (29 out of 39)
I_{DC}	< 30 mA	24 mA	58 mA	29 mA	72% (28 out of 39)
S_{11}@69 GHz	< -10 dB	-16 dB	-6 dB	-12.4 dB	90% (35 out of 39)
S_{12}@69 GHz	< -15 dB	-22 dB	-16 dB	-17.6 dB	100% (39 out of 39)

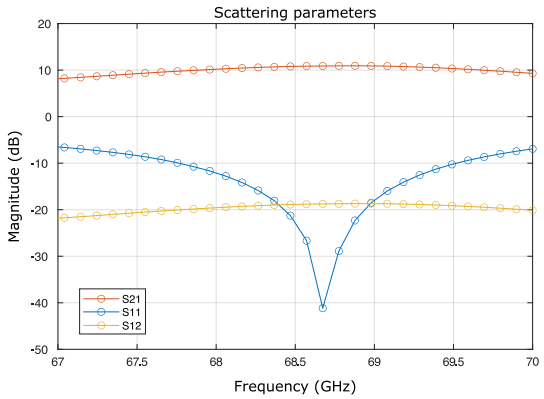

Fig. 10. Scattering parameters for a representative PA sample and nominal positions of the tuning knobs.

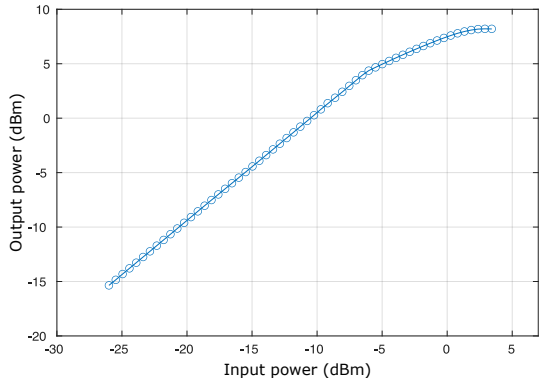

Fig. 11. Output power characteristic measured at 69 GHz for a representative PA sample and nominal positions of the tuning knobs.

rationale behind that choice is that the included calibration capabilities will be able to recover excessive yield loss without the need of overdesigning the PA to make it insensitive to process variations. In any case, even for our limited number of fabricated samples, it is clear that the fabrication yield is severely impacted by the wide performance variance due to process variations. It can be noticed that the average performance for critical specifications such as gain, saturation power, and compression point are well centered within the target performance. However, if we consider the complete set of target specifications, 37 out of the 39 fabricated samples do not comply simultaneously with all the design targets, which clearly justifies the need of a yield recovery strategy.

B. One-Shot Calibration for Yield Enhancement

To verify the feasibility and performance of the proposed machine learning-based calibration strategy, we first applied it to improve the fabrication yield of the set of fabricated PA samples. As explained before, our goal is to predict, using a machine learning regression function, the best position of the tuning knobs for each fabricated PA sample from the set of DC and low-frequency signatures generated by the process monitor circuits embedded with each PA sample. Thus, the set of DC and low-frequency signatures, S_1 to S_9, defined in Table IV was extracted for each of the 39 fabricated samples. The AC signatures associated with each nonintrusive process monitor were extracted using 50-μm GSG 145-GHz Infinity Probes from Cascade on the same VNA and probe station employed for characterizing the PA. For DC signatures, the operating point of the monitor circuits was provided through the VNA bias tee.

In high-volume production, we would use a fraction of the fabricated circuits (i.e., the training set, typically a few hundred devices) to train the machine learning prediction function (1), and then we would apply this function to recenter the performance of the rest of the produced circuits by predicting the best position of the tuning knobs. Since we only have access to 39 fabricated samples, and based on the theoretical results in Fig. 8, to provide an accurate estimation of the calibration performance we resort to a k-fold cross-validation technique to train our regression function [24]. Thus, we divided our 39 PA samples into 8 subsets (7 subsets with 5 samples and 1 subset with 4 samples). One of these subsets is kept apart as an independent verification set and the remaining samples are used as the training set to train the perceptron neural network f. For this purpose, each sample in the training set is characterized under 250 randomly generated positions of the tuning knobs, considering a variation range of $[0.6, 1]$ V for V_{B1} and V_{B2} and of $[-1, 2.5]$ V for V_{var1} to V_{var4}. Using the notation introduced in the previous section, this strategy results in 7 cross-validation folds using $N_T = 34$ samples and $N_C = 250$, and 1 cross-validation fold using $N_T = 35$ samples and $N_C = 250$.

Once the regression model for a cross-validation fold has been trained, we employ it to calibrate the performance of the samples in the corresponding verification set (i.e., the samples left out of the training set). The process is then repeated leaving out a different subset as verification set until all samples have been tuned. Notice that for the samples in the verification set, only the DC and low-frequency signatures provided by the process monitors are measured as inputs for

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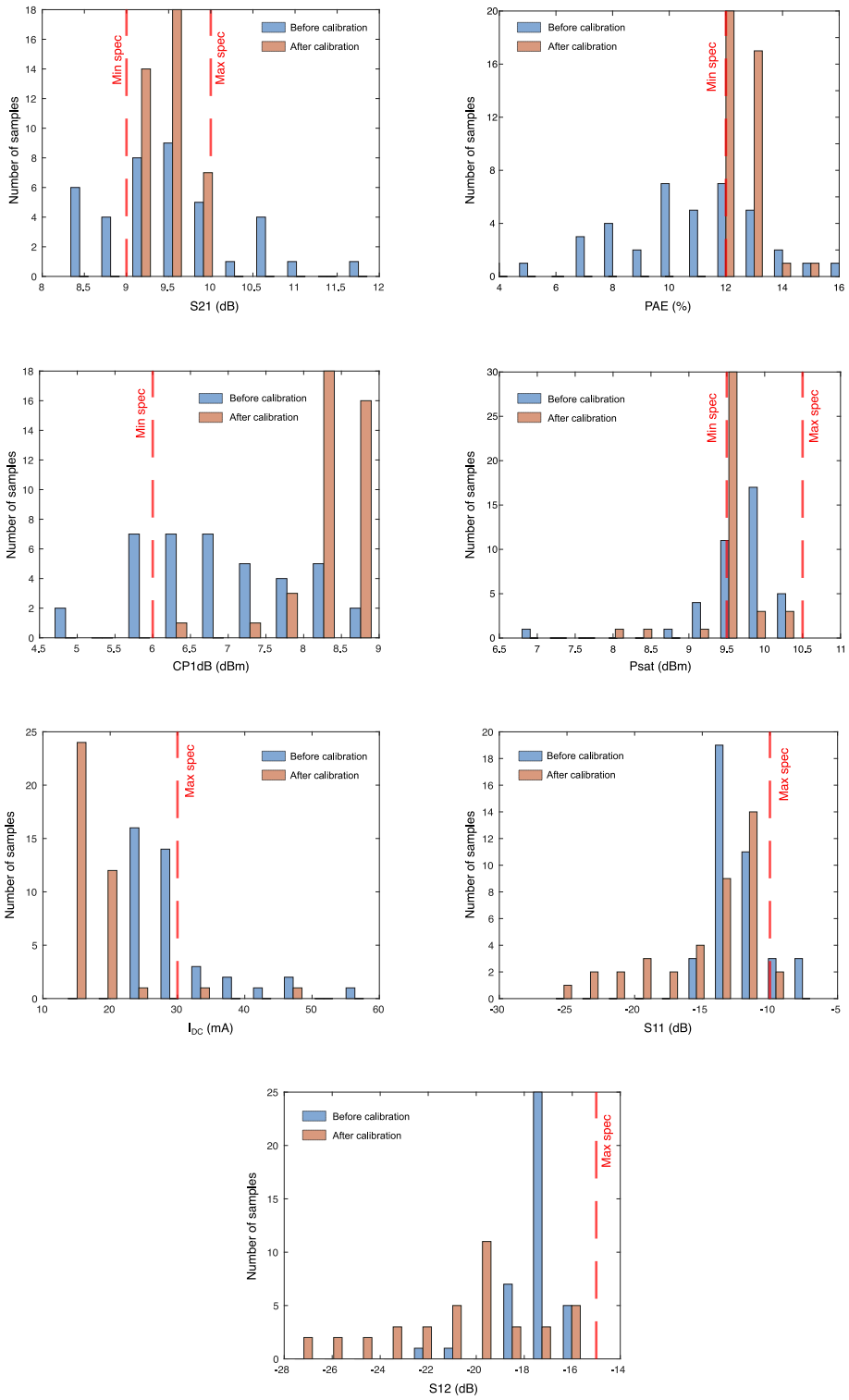

Fig. 12. Histograms of PA performance before and after calibration.

TABLE VI
PERFORMANCE SUMMARY OF THE MACHINE LEARNING-BASED CALIBRATION FUNCTION

Performance	RMS prediction error	r^2 coefficient
S_{21}@69 GHz	0.7 dB	0.90
PAE	0.8%	0.87
CP_{1dB}	0.6 dBm	0.97
P_{sat}	0.2 dBm	0.92
I_{DC}	0.4 mA	0.99
S_{11}@69 GHz	0.9 dB	0.91
S_{12}@69 GHz	0.8 dB	0.90

the calibration algorithm. As demonstrated in [23], [24], this cross-validation technique allows us to provide an accurate validation in a scenario with limited available data.

Fig. 12 shows the histograms of the PA specifications before and after calibration, obtained for the 39 fabricated samples following the described calibration procedure, together with the target specification limits. It is clear to see a dramatic increase in the fabrication yield for each of the PA specifications. Indeed, it is apparent that the calibration effectively reduces the spread of the performance distribution and centers it around the design targets. This effect is clearly observed for S_{21}, *PAE*, CP_{1dB}, P_{sat}, and I_{DC}, while the S_{11} and S_{12} parameters are optimized to comply with the design targets.

To evaluate the accuracy of the trained machine learning models linking the set of nonintrusive signatures and the tuning knob positions to the PA performance, Table VI lists the obtained Root-Mean-Square (RMS) errors for the predictions on the independent validation set, together with the square of the correlation coefficient, r^2, between the predicted and the actual performances. These two metrics are indicative of the accuracy of the proposed machine learning-based calibration and, as it can be observed, the trained machine learning model offers good predictive capabilities for the complete set of considered PA performances. It is also worth noticing that the obtained accuracy figures are in good agreement with the learning curves presented in Section IV.

Further insight can be gained by analyzing the set of optimum tuning knob values selected by the calibration algorithm. Thus, Table VII shows the min., max., average and standard deviation for the obtained optimum values of the tuning knobs, across our 39 PA samples. The wide variety observed across the different samples clearly shows that the calibration algorithm corrects sample-to-sample variations rather than a global shift (otherwise the tuning knobs would converge to a common value for all samples). This result can also be seen as a sanity check for our experiment, as it shows that we are not correcting a global shift caused by an incorrect set of initial nominal values for the tuning knobs.

The obtained yield estimations before and after calibration for the 39 fabricated samples are represented in Fig. 13 considering each individual specification and the overall specification set. The significant improvement for each of the considered PA specifications translates to an overall yield improvement from 5% (2 out of 39 samples) before calibration to 92% (36 out of 39 samples) after calibration. The obtained results demonstrate the feasibility and performance of the proposed machine learning-based calibration technique.

TABLE VII
STATISTICS OF THE OBTAINED OPTIMUM TUNING KNOB VALUES

Tuning knob	Min. (V)	Max. (V)	Average (V)	σ (V)
V_{B1}	0.6	0.875	0.79	0.1
V_{B2}	0.6	0.9	0.66	0.06
V_{var1}	-1	2.5	-0.03	0.9
V_{var2}	-1	2.5	0	0.8
V_{var3}	-1	2.5	-0.28	0.8
V_{var4}	-1	2.5	1.74	1.1

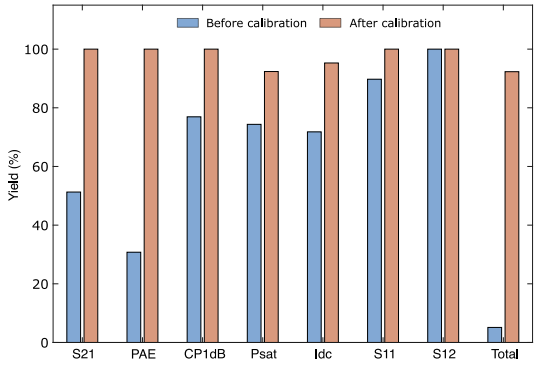

Fig. 13. Yield improvement using the proposed calibration strategy.

C. One-Shot Calibration for Design Recentering

Beyond yield enhancement applications, the proposed machine learning-based calibration also enables one-shot design recentering capabilities that may allow us to address different performance trade-offs for different application scenarios. Indeed, a different trade-off between the specifications in the PA can be targeted simply by modifying the optimization goals and/or the constraints in (2)-(3). The same machine learning function f (i.e., the function linking the position of the tuning knobs and the process monitor readings to the PA performance) can then be used to explore the tuning knob space and set the updated values corresponding to the new application scenario in one shot, without the need of an iterative search, with the only input of the set of signatures generated by the process monitor circuits.

To demonstrate the feasibility of the proposed recentering strategy, Fig. 14 represents the space of available solutions to the PA performance optimization equations (2)-(3) for three representative samples of the fabricated PA, labeled A, B, and C in the figure, obtained by exploring the tuning knob space using the machine learning function f previously trained for calibration purposes. For an easier interpretation, we represent 2-dimensional plots considering two PA specifications in each figure. Thus, Fig. 14 (a), shows the P_{sat} versus I_{DC} trade-off for the three considered samples, when all the other PA specifications comply with the nominal targets. Similarly, Fig. 14 (b) and (c) show the *PAE* and CP_{1dB} versus I_{DC} trade-offs, respectively, for the three considered PA samples. Each marker in the plots corresponds to a combination of tuning knob values that has been predicted by the proposed machine learning model from the set of process monitor readings corresponding to the considered PA sample.

From Fig. 14, a clear trade-off between PA performance and power consumption can be observed for each of the

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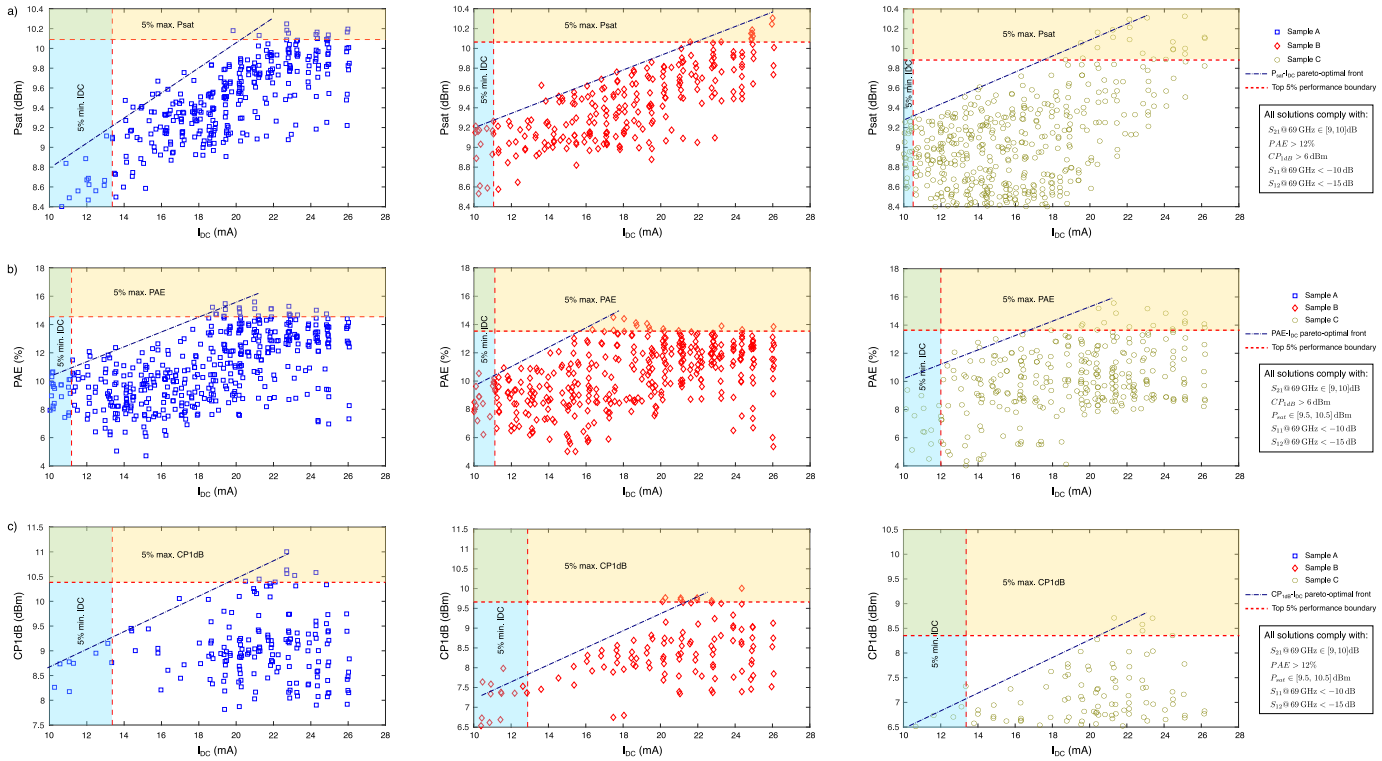

Fig. 14. Exploration of the tuning knob space and attainable performance fronts predicted by the machine learning model for three representative PA samples: a) P_{sat} vs. I_{DC} trade-off; b) *PAE* vs. I_{DC} trade-off; and c) CP_{1dB} vs. I_{DC} trade-off. Each marker corresponds to a different tuning knob combination.

considered specifications, represented in the figure by a linear approximation of the Pareto-optimal fronts for each of the considered performances. Additionally, we have highlighted the PA configurations corresponding to the 5% maximum performance for each specification and to the 5% minimum DC current consumption. This analysis illustrates the wide reconfiguration capabilities offered by the tuning knobs and justifies that they can be effectively employed for addressing different performance trade-offs. It is also worth noticing that these reconfiguration capabilities are sample-dependent, as it can be clearly ascertained by comparing the obtained results for samples A, B, and C in Fig. 14. Thus, due to sample-to-sample variations, we can observe that the DC current needed for a given performance target varies among the three samples in Fig. 14 and even the maximum attainable performance for each sample is different. In our proposed approach, the machine learning model that predicts the positions of the tuning knobs takes process variations into account by construction, as its input includes the set of signatures generated by the process monitor circuits, highly correlated to the variations of technological parameters.

To exemplify the design recentering capabilities, besides the nominal PA operation targets, we could define two aggressive goals for the calibration of the complete set of fabricated samples: a low-power operation mode with slightly degraded performance, and a high-performance operation mode with a higher power consumption. Table VIII lists the design constraints for the three proposed calibration targets for the fabricated PA: the aforementioned aggressive calibration targets aimed at minimizing power consumption and maximizing the PA performance, respectively, and the nominal calibration target already defined in the previous section. The proposed recentering technique was applied, with the constraints in Table VIII, to the set of 36 fabricated PA samples that comply with the nominal design goals after nominal calibration. Fig. 15 shows the histograms of the obtained recentering results for the set of 36 fabricated PA samples in low-power, high-performance, and nominal operation modes. It is clear to observe that the distribution of each PA performance is shifted towards the different design goals defined in Table VIII. In terms of yield, 97% of the samples (35 out of 36) are successfully recentered to the new low-power and high-performance design targets.

It is worth remembering that the only input of the calibration algorithm, besides the calibration goals, is the set of nonintrusive measurements provided by the process monitor circuits in each of the samples. The machine learning function f previously trained for nominal calibration is then readily available to predict the new combination of tuning knobs that is compatible with the new performance target, allowing in this way an easy on-the-fly performance re-tuning just by changing the calibration targets.

D. Comparison to State-of-the-Art

To better highlight our contributions, Table IX compares our work to the state-of-the-art on calibrated RF and mmW amplifiers published in the literature. Table IX is not to be read as a direct comparison between very different approaches, but it is intended to put our results into perspective. Calibration

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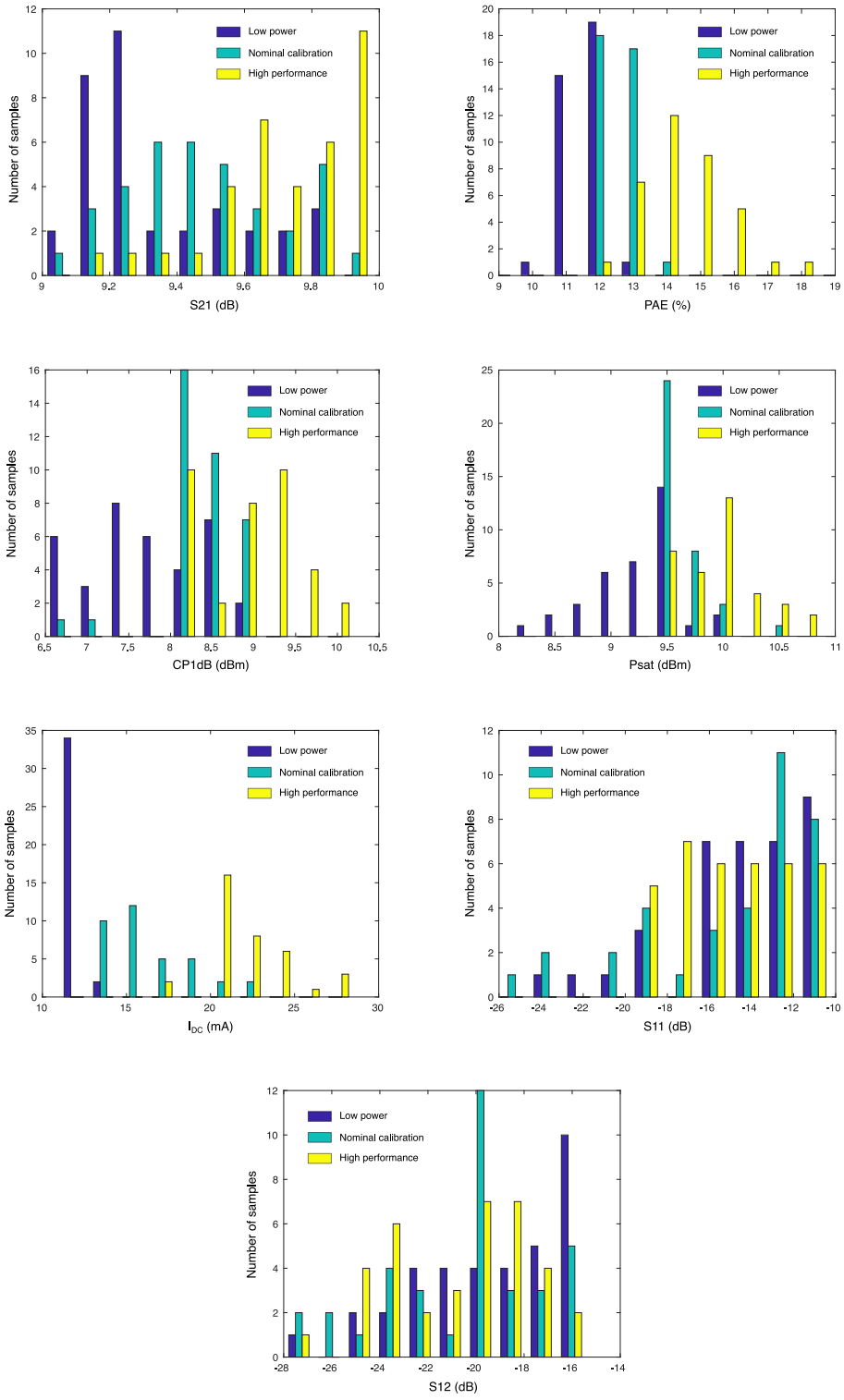

Fig. 15. Histograms of PA performance for different calibration targets: low-power operation mode (in blue), nominal operation mode (in cyan), and high-performance operation mode (in yellow).

TABLE VIII
CALIBRATION TARGETS FOR THE LOW-POWER, NOMINAL, AND HIGH-PERFORMANCE OPERATION MODES

	Low-power mode	**Nominal calibration**	**High-performance mode**
S_{21}@69 GHz	$\in [9,\ 10]$ dB	$\in [9,\ 10]$ dB	$\in [9,\ 10]$ dB
PAE	$> 10\%$	$> 12\%$	maximize, $> 13\%$
CP_{1dB}	> 6 dBm	> 6 dBm	maximize, > 8 dBm
P_{sat}	> 8 dBm	$\in [9.5,\ 10.5]$ dBm	maximize, > 9.5 dBm
I_{DC}	< 15 mA	< 30 mA	< 30 mA
S_{11}@69 GHz	< -10 dB	< -10 dB	< -10 dB
S_{12}@69 GHz	< -15 dB	< -15 dB	< -15 dB

approaches for LNAs and PAs are considered, as the general calibration principles are similar even if the functions of these two circuits are different in nature. Compared to the state-of-the-art, our work presents a very low design complexity. Since we rely on nonintrusive process monitors to guide the calibration and tunable decoupling capacitors and bias voltages as tuning knobs, we avoid circuit-specific architectures and complex co-design that may require deep modifications on the circuit under calibration. The fact that all required measurements are DC or low-frequency measurements and that no high-frequency test stimulus is required greatly relaxes the test requirements.

The proposed calibration strategy also seems particularly suitable for multidimensional problems. As it can be seen in Table IX, most of the previously published calibration strategies are limited to less than 4 simultaneously corrected parameters, while our proposed strategy demonstrated the simultaneous correction of 7 performance parameters. This is due to the multidimensional nature of the machine learning-based performance monitoring and correction algorithm, which takes into account the complex multi-variate dependencies between nonintrusive signatures, tuning knobs, and performance parameters.

It is also worth noticing that experimental validations based on a significant number of fabricated samples remain rare in the existing literature. In this regard, our proposal is demonstrated in a set of 39 fabricated samples, that, although far from high-volume fabrication numbers, is a valuable contribution in the light of the existing literature.

On the other hand, as a disadvantage compared to other published approaches, self-healing applications, for instance, targeting temperature or aging compensation, are not possible with the proposed strategy. Adapting the proposed calibration technique to self-healing would require adding on-chip instruments to monitor some critical nodes of the circuit under calibration.

VI. CONCLUSION

We have experimentally validated a machine learning-based calibration methodology for mm-wave integrated PAs. The proposed calibration strategy employs a one-shot statistical calibration technique guided by nonintrusive process monitors. The developed calibration algorithm is able to predict the best position of the tuning knobs for reaching a predefined calibration target, without the need for a test-and-tune iterative loop.

A 69 GHz PA with one-shot calibration capabilities has been designed and fabricated in STMicroelectronics 55 nm CMOS technology. The proposed PA includes five on-chip process monitor circuits for nonintrusive performance monitoring and integrates a generic tuning knob based on variable decoupling capacitors. Experimental results on 39 fabricated samples of the proposed PA demonstrate the feasibility and performance of the proposed calibration methodology. Two experimental scenarios are considered. The first one aims at improving fabrication yield by compensating performance degradation due to excessive process variations, while the second one is aimed at recentering the fabricated PA performance by considering aggressive calibration targets far from the nominal design. Regarding yield enhancement, obtained results show that the proposed strategy dramatically reduces the impact of process variations, significantly improving the PA performance of individual samples and the overall fabrication yield. Recentering applications, on the other hand, are demonstrated by considering two opposite performance trade-offs: one targeting high-performance operation at the cost of power consumption and another targeting low-power operation at the cost of a slightly degraded performance.

Compared to the current state-of-the-art, the proposed calibration circuitry has the advantages of not requiring the tuning of the power supply and not loading the nodes of the PA with embedded test instruments, avoiding this way complex co-design. Moreover, performance monitoring is achieved by indirect DC and low-frequency signatures, relaxing this way the requirements on the test equipment. As a disadvantage, the price to pay for the simplicity of the proposed approach is that it is not suitable for self-healing applications, since the process monitor circuits do not track degradations of the actual PA circuitry. Future research in this line may target an extension to self-healing applications by including additional on-chip resources to monitor key internal nodes in the PA circuitry and exploring the application of the proposed techniques to different PA architectures.

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TABLE IX
COMPARISON TO THE STATE-OF-THE-ART ON CALIBRATED RF AND MMW AMPLIFIERS

Ref.	Highlights	Validation	Advantages	Disadvantages
[8]	· One-shot calibration · Calibration of S-parameters · On-chip ring oscillator for stimulus generation · On-chip peak detector for performance monitoring · Tuning knobs: supply voltage and bias voltages	· 1.57 GHz LNA · Experimental results: 144 devices	· No need of test-and-tune iterations	· Limited to S-parameters · No calibration of nonlinearities, NF · Modification of power supply voltage · Complexity of added on-chip circuitry
[9]	· One-shot calibration · Calibration of S-parameters and NF · On-chip ring oscillator for stimulus generation · On-chip peak detector for performance monitoring · Tuning knobs: supply voltage and bias voltages	· 1.57 GHz LNA · Monte Carlo simulations	· No need of test-and-tune iterations	· No calibration of nonlinearities · Validated by simulation · Modification of power supply voltage · Complexity of added on-chip circuitry
[10]	· Test-and-tune calibration · Calibration of S_{21}, NF, I_{DC} and $IP3$ · External optimized test stimulus · On-chip envelope detector for performance monitoring · Tuning knobs: bias voltage and PMOS IMD sinker	· 1.9 GHz LNA · Monte Carlo simulations · Experimental results: 3 devices	· Low-frequency indirect measurements	· Iterative calibration · Validated by simulation · Complex external stimulus · Circuit-specific tuning solution
[12]	· Calibration based on reinforcement learning · Optimization of PAE and linear gain region	· Doherty PA · Behavioral simulation	· Self-learning calibration algorithm	· Validated by behavioral simulation · No practical implementation
[14]	· One-shot calibration · Calibration of S_{21}, I_{DC}, PAE, CP_{1dB} · Nonintrusive sensors · Tuning knobs: independent power supplies and bias voltages	· 2.4 GHz PA · Experimental results: 55 devices	· No need of test-and-tune iterations · Nonintrusive performance sensing · Low-frequency and DC indirect measurements	· Modification of power supply voltage · Requires multiple power supply domains · Not suitable for self-healing
[17]	· Test-and-tune calibration and self-healing · Calibration of P_{sat}, PAE, S_{21} and 4:1 VSWR tolerance · On-chip DC current, RF power, and temperature sensors · Tuning knobs: Tunable transmission line stubs and bias voltages	· 28 GHz PA · Experimental results: 20 devices	· Demonstrates yield enhancement and self-healing · Fully integrated solution	· Iterative calibration · Complexity of added on-chip circuitry
[18]	· Test-and-tune calibration · Calibration of S_{21} and S_{11} · On-chip power detector · Tuning knobs: Tunable transmission line stubs	· 56 GHz PA · Experimental results: 1 device	· Suitable for self-healing	· Iterative calibration · Complexity of added on-chip circuitry · Only 1 device, no statistical data
[19]	· Test-and-tune calibration · Calibration of NF and power consumption · On-chip temperature and DC voltage sensors · Tuning knobs: Tunable transmission lines and bias currents	· 60 GHz LNA · Experimental results: 9 devices	· Calibration and self-healing of PVT variations · Fully integrated solution · Indirect DC measurements	· Iterative calibration · Only NF and power are calibrated
[20]	· Test-and-tune calibration · Calibration of Gain, PAE, $OIM3$ · Output power sensing · Tuning knobs: tunable feedback loop	· 60 GHz PA · Experimental results: 10 devices	· Calibration and self-healing capabilities	· Iterative calibration · External stimulus needed · Complex added circuitry · Tailored to specific PA architecture
This work	· One-shot calibration · Calibration of S_{21}, S_{12}, S_{11}, I_{DC}, P_{sat}, CP_{1dB}, PAE · Nonintrusive sensors · Tuning knobs: variable decoupling capacitor and bias voltages	· 69 GHz PA · Experimental results: 39 devices	· No need of test-and-tune iterations · Nonintrusive performance sensing · DC and low-frequency indirect measurements · No modification of power supplies · Generic nonintrusive sensors and tuning knobs · Demonstrates yield enhancement and design recentering	· Not suitable for self-healing

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