Channel-Width-Dependent Mobility Degradation in Bulk Conduction Regime of Tri-Gate Junctionless Transistors

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Channel-width dependent mobility degradation in bulk conduction regime of tri-gate junctionless transistors

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***Abstract*—Junctionless transistors (JLTs) have promising strengths such as extremely simple structures without p-n junctions, better reliability and low flicker noise, for overcoming scaling challenges for advanced sub-5nm nodes. In this paper, channel-width dependent operation in partially depleted regime of tri-gate JLTs were investigated with comparison to conduction in conventional inversion-mode (IM) transistors. A large difference of transconductance (g_m) against gate-to-channel capacitance (C_{gc}), and the reduced amplitude of first peak on dg_m/dV_g were identified under the partially depleted regime in JLTs, due to a severe transverse E-field near threshold voltage (V_{th}). However, the impact of E-field was weakened as decreasing channel-width of JLTs. These works provide a key information for better understanding channel-width dependent performance of JLTs and for implementing practical applications with them.**

***Index Terms*—Channel-width dependence, nanowire (NW)-like structure, partially depleted regime, peaks on dg_m/dV_g, tri-gate junctionless transistors (JLTs), transconductance (g_m) degradation, transverse electric-field (E-field).**

I. Introduction

FURTHER scaling down of transistors is continuously required in the fourth industrial revolution era, explained by Internet of Things (IoT), artificial intelligence (AI), mobile devices and big data with cloud computing [1]. A number of efforts, in terms of gate stack, strain engineering, 3-dimensional structures and alternative channel materials, have been suggested to fulfill power, performance, area and cost with minimizing short channel effects (SCEs) [2-5]. Recently, junctionless transistors (JLTs) have received considerable attention to overcome scaling challenges for advanced sub-5nm nodes. Extremely simple structures without p-n-junctions, better reliability and lower flicker noise are key advantages of JLTs [7-15]. An additional implantation process on source and drain regions can also improve performance of JLTs with reducing access resistance [16]. In addition, advanced transistors with excellent short-channel characteristics, high-performance sensors and multifunctional devices have been implemented as JLTs with a variety of materials, including polycrystalline silicon (Si), III–V semiconductors, and 2-D transition metal dichalcogenides (TMDs) [7].

In this paper, the channel-width influenced operation in partially depleted regime of JLTs were investigated in detail. Behavior of bulk conduction near threshold voltage (V_{th}) of planar-like JLTs was more affected by transverse electric-field (E-field), than conduction in conventional inversion-mode (IM) transistors. However, the impact of E-field near V_{th} was mitigated in nanowire (NW)-like JLTs due to effects of sidewall gates. Consistent results were also shown in temperature dependence of electrical properties in JLTs and numerical simulation works.

II. Experiments

JLTs were fabricated at CEA-Leti on (100) SOI wafers with device Si ≈ 9.2 nm, high-k dielectric ≈ 1.2 nm and thick buried oxide (BOX) ≈ 145 nm. JLT channel was highly doped with phosphorus targeted at $10^{19}/cm^3$, and IM transistors were also fabricated by the same process only except for channel doping concentration. Further detail processes for device fabrication and material parameters were explained in previous works [17,18]. Current-voltage characteristics with varying temperatures from 80 K to 350 K were measured by using HP 4155A semiconductor parameter analyzer, and HP4294a with a 50 mV small signal at 500 kHz was used for getting capacitance-voltage characteristics. In case of gate-to-channel capacitance (C_{gc}) measurements of NW-like JLTs, devices with very long gate-length (L = 10 μm) were selected in arrays of 50 channels, for a better accuracy with minimizing contact resistance effect and mobility degradation induced by drain-bias. In addition, FlexPDE software based on finite element models was used for obtaining simulated results.

III. Discussion

Figure 1(a) and 1(b) show gate-to-channel capacitance (C_{gc}), its derivative (dC_{gc}/dV_g), corresponding transconductance (g_m) and dg_m/dV_g of a planar-like IM transistor with a long

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gate-length (L = 10 µm), respectively. The C_{gc} and dC_{gc}/dV_g characteristics are theoretically equivalent to g_m and dg_m/dV_g ones, except that there are no mobility degradation effects, mainly resulting from transverse E-field, nor series resistance effects in the capacitance-based characteristics [19].

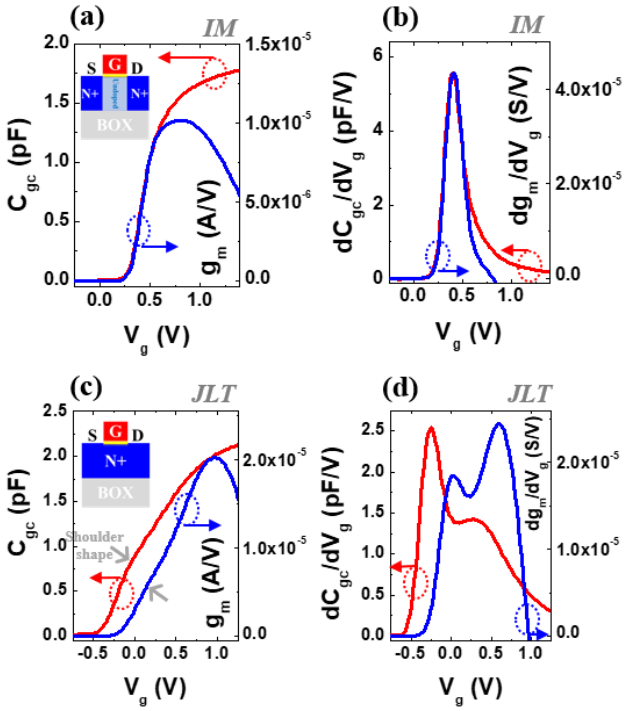

Fig. 1. (a) Measured C_{gc}, g_m, (b) dC_{gc}/dV_g and dg_m/dV_g of a planar-like IM transistor (L = W = 10 µm) as illustrated in Fig. 1(a). (c) Measured C_{gc}, g_m, (d) dC_{gc}/dV_g and dg_m/dV_g of a planar-like JLT (L = W = 10 µm) as illustrated in Fig. 1(c). The devices were biased in the linear operation regime with V_d = 20 mV at T = 300 K.

As V_g was increased, C_{gc} in the red curve of Fig. 1(a) started to increase as a result of the formation of inversion channel, then reached a maximum value, which denotes capacitance of gate-insulator. The dC_{gc}/dV_g plot in Fig. 1(b) also showed a single peak meaning threshold voltage ($V_{th} \approx 0.4$ V). The behavior of g_m and dg_m/dV_g near V_{th} was very consistent to that of C_{gc} and dC_{gc}/dV_g, while a significant degradation of g_m was observed for further increasing V_g (> 0.75 V) due to surface roughness scattering [20]. In addition, the C_{gc}, dC_{gc}/dV_g, g_m and dg_m/dV_g curves of a planar-like JLT with the same geometry were plotted in Fig. 1(c) and 1(d). A shoulder shape on C_{gc} and two clear peaks on dC_{gc}/dV_g, positioned at threshold voltage (V_{th}) and at flat-band voltage (V_{fb}), were clearly observed. They are typical of JLTs, as a manifestation of bulk channel conduction [7,18]. Compared with IM devices, less g_m degradation at large V_g (> 0.75 V) was observed in Fig. 1(c) consistently with previous results [21,22]. However, near V_{th}, the C_{gc} and g_m plots of the JLT were displaying very different behaviors. In particular, g_m displayed a much smaller shoulder than C_{gc} and the two peaks observed on dC_{gc}/dV_g and dg_m/dV_g characteristics displayed inverse relative amplitudes. Such discrepancies could be due to a non-uniform distribution of point defects in the JLT channel [23], and a severe transverse E-field during operation near $V_g = V_{th}$.

Temperature dependent g_m of the planar-like IM transistor was plotted as a function of gate voltage overdrive ($V_g - V_{th}$) as shown in Fig. 2 (a). V_{th} with varying temperature was determined by using the constant current technique at $I_d \times L/W \approx 10^{-7}$ A. It is well known as g_m is strongly related to the trend of effective mobility (μ_{eff}), and temperature dependent μ_{eff} can be given by an empirical mobility model based on Matthiessen's rule as [24,25]:

$$\frac{1}{\mu_{eff}(T)} = \frac{1}{\frac{300}{T}\times ph} + \frac{1}{\frac{T}{300}\times C} + \frac{1}{neu} + \frac{1}{sr} \quad (1)$$

where ph, C, neu and sr denote μ_{eff}-contributions resulted from phonon scattering, Coulomb scattering, neutral defect scattering and surface roughness scattering, respectively. Normalized g_m near V_{th} in Fig. 2(b) tended to increase as decreasing temperature, indicating acoustic phonon-dominated scattering. Figure 2(c) showed temperature dependence of g_m in the planar-like JLT. A typical phonon scattering governed behavior was identified for the regime of $V_g - V_{th} > 0.5$ V. However, the value of g_m near V_{th} seemed not to change about the temperature variation. Indeed, the normalized g_m in Fig. 2(d) was slightly changed only by varying temperature due to temperature independent surface roughness (SR) scattering as well as defect-induced scattering [26,27]. A SR-like scattering of charge carriers can be induced between bulk neutral channel and depletion area in JLT by a considerable transverse E-field in the partially depleted operation-regime.

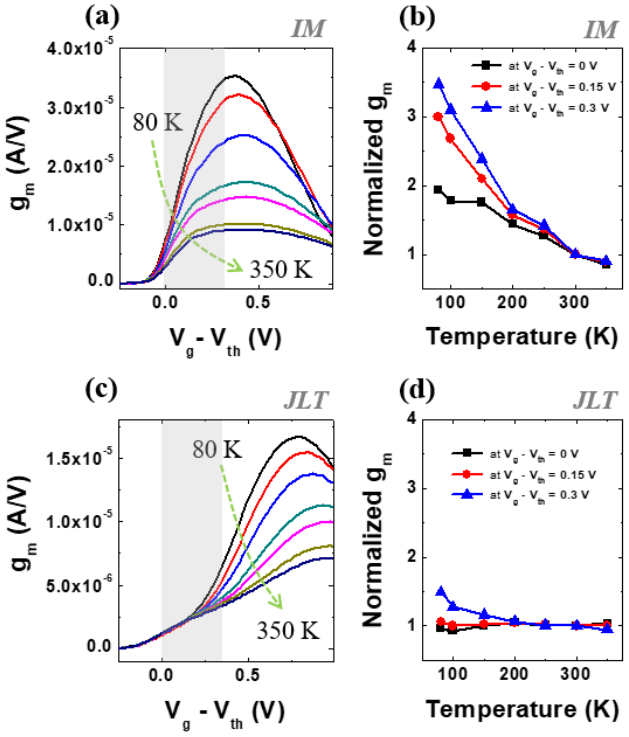

Fig. 2. (a) Temperature dependent g_m, and (b) normalized g_m near V_{th} as marked in gray of Fig. 2(a) versus temperature of planar-like IM transistor. (c) Temperature dependent g_m, and (d) normalized g_m near

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V_{th} as marked in gray of Fig. 2(c) versus temperature of planar-like JLT. The devices were biased in the linear operation regime with V_d = 20 mV.

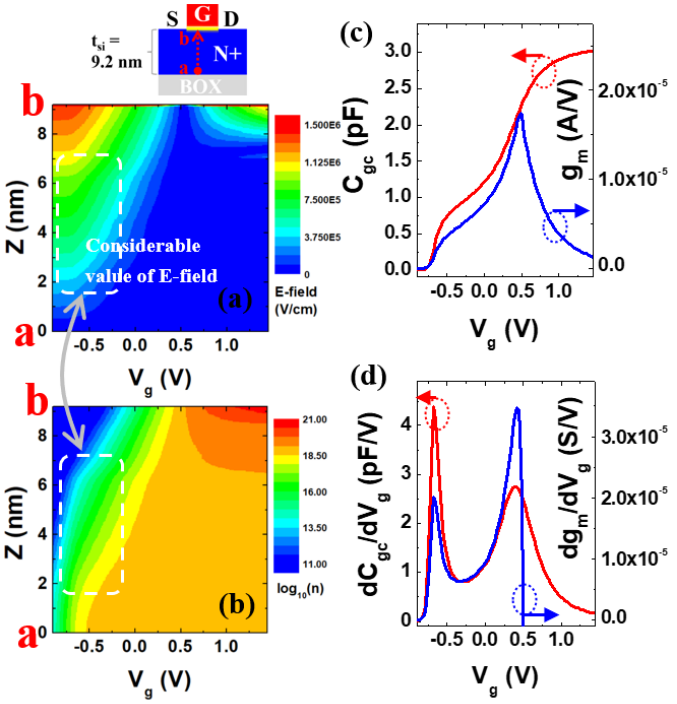

Fig. 3. (a) Simulated distribution of transverse E-field and (b) charge carrier concentration (n), across the JLT channel (from bottom interface 'a' to top interface 'b' in the illustration). The ordinate z refers to the distance from bottom Si/BOX interface. The evolution of these distributions is shown as a function of V_g, in abscissa. (c) Corresponding plots of C_{gc}, g_m, (d) dC_{gc}/dV_g and dg_m/dV_g.

The variation of transverse electric field (E-field) and charge carrier concentration (n), along the cutline a-b which goes from bottom to top interface across the JLT channel, is mapped against V_g in Fig. 3(a) and 3(b), respectively [12]. Depending on V_g, there are two conduction regimes in JLTs, with bulk conduction for $V_{th} < V_g < V_{fb}$ and surface accumulation for $V_g > V_{fb}$. Transverse E-field at the interface between Si channel and gate-insulator is getting reduced as decreasing V_g, and then, the magnitude of the E-field is theoretically zero when V_g reaches V_{fb}. Moreover, for further decreasing V_g, the E-field is reinforced again in the partial depletion-state of JLT [21,23]. For $V_g = V_{fb}$ (≈ 0.5 V), effectively zero E-field throughout the JLT channel was verified in blue as shown in Fig. 3(a), and whole JLT channel is full of charge carriers with $\log_{10}(n) = 19$ in orange color in Fig. 3(b). As decreasing $V_g < V_{fb}$, the value of E-field is getting increased from the top interface, and these give rise to the depletion of charge carriers. Therefore, degradation of bulk channel mobility in the partially depleted regime of JLT can occur, since electron charge carriers at $V_{th} < V_g < V_{fb}$ are influenced by considerable value of E-field as indicated in the white dotted line of Fig. 3(a) and 3(b). Corresponding C_{gc}, dC_{gc}/dV_g, g_m and dg_m/dV_g were plotted in Fig. 3(c) and 3(d). The g_m was simulated with considering a transverse E-field affected mobility (μ_{field}) as [28]:

$$\mu_{field} = \frac{\mu_0}{1+\left(\frac{E_{eff}}{E_c}\right)^{\alpha}} \qquad (2)$$

where μ_0, E_{eff}, E_c and α denote low-field mobility (= 150 cm^2/Vs), effective transverse E-field, critical E-field (= 5×10^5 V/cm) and the mobility attenuation exponent (= 1.5), respectively. Mobility degradation with respect to non-uniform defects in the channel was also taken into account with following equation [29]:

$$\mu_0 = \mu_{back0} + (\mu_{top0} - \mu_{back0}) \times \frac{y}{t_{si}}, \quad [0 \le y \le t_{si}] \qquad (3)$$

where μ_{top0} and μ_{back0} are low-field mobility at top interface (= 150 cm^2/Vs) and bottom interface (= 100 cm^2/Vs), individually. Similar behavior to the experimental results in Fig. 1(c), such as clearly reduced shoulder shape, was investigated in Fig. 3(c). Trend of relative amplitude-ratio between first and second peak on dC_{gc}/dV_g and dg_m/dV_g in Fig. 3(d) was also consistent to that in Fig. 1(d).

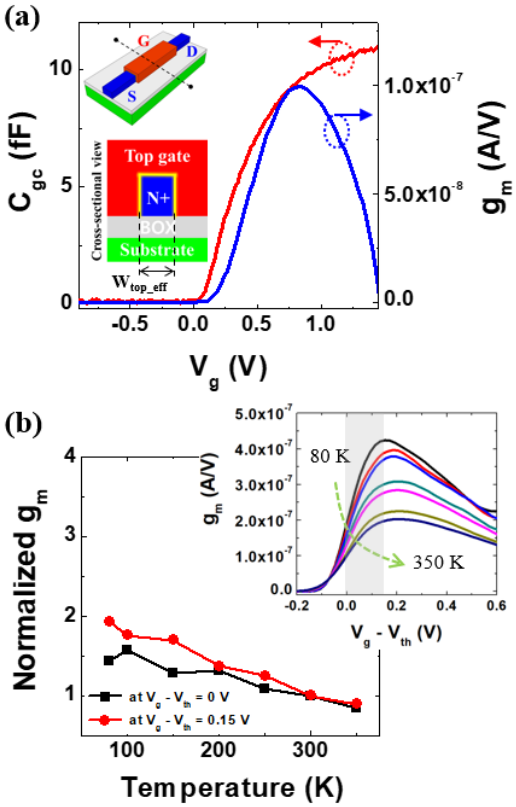

Fig. 4. (a) Measured C_{gc} and g_m of a NW-like JLT (W_{top_eff} ≈ 25 nm, L = 10 μm), as described in the illustration (T = 300 K). (b) Normalized g_m near V_{th} as marked in gray of the inset versus temperature of the NW-like JLT. The device was biased in the linear operation regime with V_d = 50 mV.

Figure 4(a) shows the measured C_{gc} and g_m of a NW-like JLT with top-effective width (W_{top_eff}) ≈ 25 nm. Shoulder shape near V_{th} was vanished due to the shrunk portion of bulk neutral channel as compared to surface accumulation channel, and

enhanced sidewall gate effects [30]. In addition, difference between C_{gc} and g_m for 0 V < V_g < 0.5 V (the partial depletion-state) has significantly narrowed as compared to the results from the planar-like JLT in Fig. 1(c). Normalized g_m near V_{th} was also increased as decreasing temperature in Fig. 4(b). One can expect that SR scattering is reduced and then, impact of phonon scattering is relatively getting stronger in the operating regime of NW-like JLT.

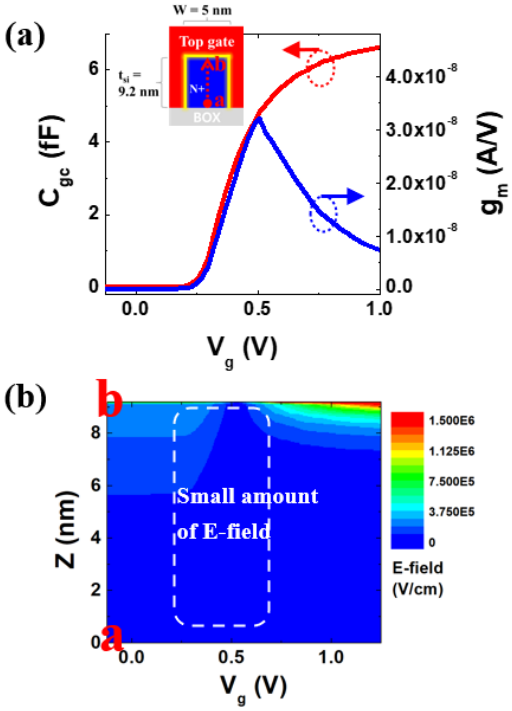

Fig. 5. (a) Simulated C_{gc} and g_m of a NW-like JLT (W = 5 nm, L = 10 µm and V_d = 50 mV). (b) Corresponding distribution of transverse E-field, across the NW-like JLT channel from bottom interface 'a' to top interface 'b' in the illustration of Fig. 5(a). The ordinate z refers to the distance from bottom Si/BOX interface.

Simulated C_{gc} and g_m of a NW-like JLT with W = 5 nm and L = 10 µm were plotted in Fig. 5(a). Corresponding distribution of transverse E-field was also shown in Fig. 5(b) [30]. Indeed, only a slight variation between C_{gc} and g_m shape was observed for 0.25 V < V_g < 0.5 V, and magnitude of transverse E-field was negligible in that operating regime, as identified in the white dotted line of Fig. 5(b). Sidewall gate effects in the NW structures cause the weakened SR scattering in the partially depleted operation. Furthermore, as the width of tri-gate JLTs decreases, V_{th} position is getting closer to V_{fb} [30,31]. Even from this point of view, the reduced E-field effects and less degradation of g_m near V_{th} in the NW-like JLTs is quite reasonable.

IV. Conclusion

Channel-width dependent behavior of bulk conduction in JLTs were investigated for the first time. Even though less transconductance (g_m) degradation for a strong accumulation-operation in JLTs was observed as compared to that of inversion-mode (IM) transistors, the reduced amplitude of first peak on dg_m/dV_g, and a large variation between C_{gc} and g_m near V_{th} operation-regime were shown in JLTs, since a severe transverse E-field under the partially depleted operation. However, weakened E-field effects and less degradation of g_m near V_{th} were identified in nanowire (NW)-like JLTs, due to impact of sidewall gates in the narrow structures. Those results were also verified by temperature dependence of g_m behavior, and numerical simulation about distribution of transverse E-field and charge carrier concentration in JLT channel. In addition, a significant V_{th} variation with changing width of tri-gate JLTs [30,31] can be explained well by the results.

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