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Abstract

Scalable fabrication of Si nanowires with a critical dimension of about 100 nm is essential to a variety of applications. Current techniques used to reach these dimensions often involve e-beam lithography or DUV lithography combined with resolution enhancement techniques. In this study, we report the fabrication of <150nm Si nanowires from SOI substrates using DUV lithography (λ = 248 nm) by adjusting the exposure dose. Irregular resist profiles generated by in-plane interference under masking patterns of width 800 nm were optimized to split the resulting features into twin Si nanowires. However, masking patterns of micrometre size or more on the same photomask does not generate split features. The resulting resist profiles are verified by optical lithography computer simulation based on Huygens-Fresnel diffraction theory. Photolithography simulation results validate that the key factors in the fabrication of subwavelength nanostructures are the air gap value and the photoresist thickness. This enables the parallel top-down fabrication of Si nanowires and nanoribbons in a single DUV lithography step as a rapid and inexpensive alternative to conventional e-beam techniques.

Keywords: photolithography, deep ultraviolet, silicon on insulator, nanowire

1. Introduction

Si nanowires (NW) are used in a variety of applications, including the recent research on field-effect transistor (FET) sensors, in particular on biosensors [1]–[4], due to their high surface-to-volume ratio and electron mobility. Alternative structures like Si nanoribbons (NR) can efficiently replace NWs in such sensing applications, where lateral critical dimension (CD) is not a crucial parameter [5]–[8]. Top-down fabricated Si NWs are generally preferred over bottom-up NWs because of their compatibility with CMOS technology. However, achieving feature sizes of 100 nm and below is still challenging without industry-grade equipment, and generally requires costly e-beam lithography processes or the combination of deep-UV (DUV) lithography with size reduction methods. Methods for reducing the size of Si NWs include the use of spacers and sacrificial layers [9], mesa isolation techniques, controlled anisotropic etching [1], [10], resist trimming, or thinning down Si features through cycles of thermal oxidation and selective oxide etch. These methods extend the resolution limits of lithography and can result in feature sizes down to about 10 nm, potentially. However, some of these methods are not compatible with silicon-on-insulator (SOI) substrates, which are playing a growing role in advanced CMOS processes.

Here, we present an alternative fabrication method of Si NWs from SOI substrates using DUV lithography. By taking advantage of in-plane interference and adjusting exposure parameters, it is possible to generate ridged resist features resulting in isolated twin NWs and to reach sub-wavelength CD. Interference between the incident wave and the reflected wave due to substrate reflectivity can generate vertical standing-wave roughness on resist sidewalls [11] and is generally suppressed by adding a bottom anti-reflective coating (BARC) to the resist stack [12]. In-plane interference is used in laser interference lithography (LIL) as a maskless technique to generate periodic nanodot or nanowire patterns on a large scale [13]–[15]. In this study, isolated horizontal interference patterns were observed, inducing wave variations in the resist profile, and were exploited to split Si features into twin NWs. Nanowires with a CD down to 120 nm were successfully fabricated from 800 nm mask pattern in a single step, without any thinning process, by optimizing the exposure dose. This method allows fast prototyping and scalable fabrication of NWs and NRs without the need for expensive and time-consuming e-beam lithography. Extensive optical lithography numerical simulation is conducted by ATHENA's Optolith (Silvaco) in which the experimental process flow of fabrication is respected. The simulation results confirm that the air gap value (between the mask patterns and the photoresist surface), photoresist thickness and the mask patterns width are the key factors allowing the introduction of diffractions in the conventional DUV lithography process.

2. Materials and methods

SOI substrates with 70-nm-thin single-crystal Si film and 145-nm-thin buried oxide were spin-coated by UV5 (Microchemicals) positive photoresist (PR) at 4000 rpm for an expected thickness of about 0.525 µm, and baked for 60 s at 130 °C. Substrates were aligned with a quartz/chrome mask holding linear patterns of widths 0.8, 1.0 and 1.3 µm using a Süss Microtech MJB4 mask aligner in vacuum contact mode. The samples were exposed for 1 s by a Hg/Xe deep-UV (DUV) source with a nominal power of 4 $mW.cm^{-2}$ at wavelength 248 nm.

For optimization purposes, as will be discussed further, the exposure time ranged from 0.9 to 2.6 s. A post-exposure bake was applied for 90 s at 130 °C before the samples were bathed in AZ326MIF developer and rinsed with DIW. The topmost Si film was etched by SF_6 reactive ionic etching (RIE) using a Corial 200 IL RIE, and etch depth was controlled by end-point detection (EPD). Resist stripping was then conducted with AR300-76 remover and the surface was cleaned by oxygen plasma.

3. Results

Exposure parameters for DUV lithography were initially adapted from standard Si processes to be used on SOI substrates. Conformity of the resulting PR and Si patterns to the target dimensions was controlled on bulk Si substrates using the same parameters. However, on SOI substrates, it is noticeable that resist patterns are not correctly resolved. The overall footprint of the linear patterns is wider than the expected 0.8, 1.0 and 1.3 µm. As shown on Figure 1a and 1b, the resist features have curved lateral walls, inclined with an angle of about 75° with the surface, and a ridged cross-section split by a groove in the middle.

The feature shown in Figure 1awas obtained using UV5 resist and exposing it for 1.3 s, which was the standard for Si. Since it is a positive resist, the middle groove indicates a partially overexposed area centred underneath opaque chrome patterns. The spatial profile of resist features provides information about the actual distribution of light intensity in the resist volume compared to the expected amplitude generated by the masking patterns, as illustrated in Figure 1b. The cross-sectional shape can also be found in the plane of the Si surface, as parabolic lobes are formed instead of right angles.

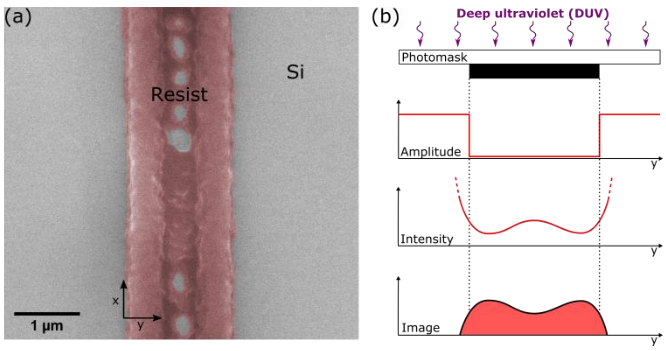

Figure 1. (a) Top-view SEM images of typical resist features obtained by deep-UV lithography of a linear pattern of 1.3 µm width on 70/145 nm SOI substrates. The photoresist is colourized in red. (b) Schematic cross-section view of the light profile under a chrome pattern and the resulting positive PR feature.

The morphology of resist features was investigated using SEM with variable target width. Figure 2 shows the resist image of crossed linear mask patterns, which range from 0.8 to 2 µm in width. The exposure time was fixed at 2 s to deliver a dose of 8 $mJ.cm^{-2}$. SEM images show that the middle groove is almost absent from 2 µm patterns and becomes deeper and wider as the target width decreases, until the total splitting of the features under 1 µm. The peak resist thickness on isolated lines ranges from 0.5 µm for wide lines down to about 0.1 µm for split nanolignes. Regarding the measured width, patterns of width 1.6 µm and more appear to be transferred with high fidelity, whereas smaller patterns generate a footprint of limit width 1.4 µm approximately.

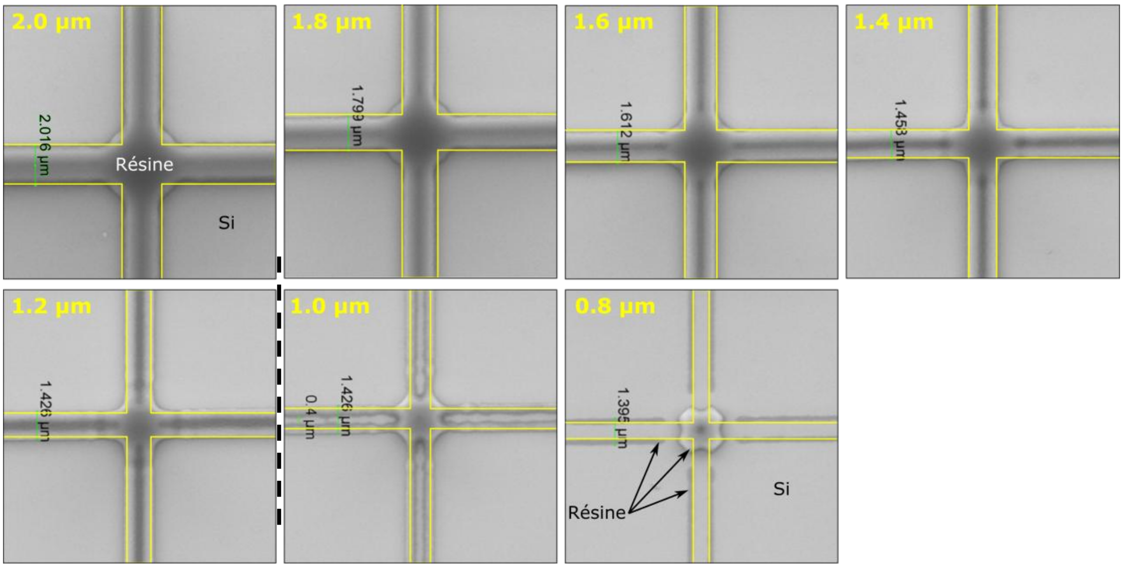

Figure 2. Top-view SEM images of UV5 resist features formed on an SOI substrate from intersecting mask patterns, with a width ranging from 0.8 to 2.0 µm, using DUV lithography (248 nm) at an exposure dose 8 mJ.cm^{-2}. Target patterns are drawn as yellow frames.

The results presented above indicate that the resist profile varies non-linearly with the Cr mask pattern width at a set exposure dose. In this case, a critical target width between 1.0 and 1.2 µm represents the "splitting threshold" where the centre groove due to induced exposure is deep enough to reach the substrate. This threshold is illustrated as a dashed line in Figure 2.

The influence of exposure dose was also conducted to optimize process parameters. Several samples coated with PR of the same thickness were exposed for 1 to 2.6 s with a surface power density fixed at 4 mW.cm^{-2}. All other process parameters were identical between the samples and the resulting resist features after development was studied by SEM.

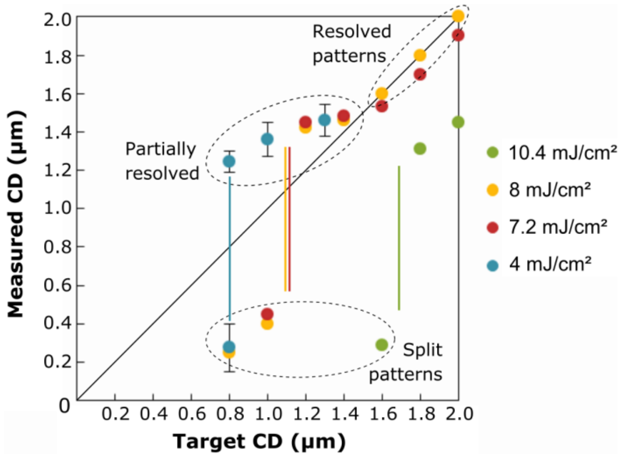

Figure 3. Average measured critical dimension (CD) of resist features as a function of mask target CD for different exposure doses of UV5 resist on SOI. Error bars correspond to the standard deviation, based on the measurements of about 100 nanostructures obtained with the optimal experimental dose.

Figure 3 shows the plot of the average measured critical dimension (CD) as a function of target width, for different exposure doses. A single mask pattern may result in whole resist features or split ones. In this case, the resulting CDs are displayed as two separate populations, as can be seen at CD_{target} = 0.8 µm for the sample exposed by 4 mJ.cm^{-2}.

Results show that the actual resist width varies non-linearly as a function of target width along with the mask patterns' range. Only the largest targets (CD > 1.5 µm) are resolved accurately with a moderate exposure dose of 7–8 mJ.cm^{-2}. With a larger dose, a bigger volume of resist is made soluble to the developer and thus the patterns are reasonably narrower. Oppositely, under-exposure results in wider resist patterns. However, under a critical target width of about 1.5 µm, data no longer fits with the bisector line as the resist features displayed a wider footprint than expected. These partially resolved features do result as single lines of resist, but with a linewidth print bias and a deep central groove which may produce holes on silicon. When the target width is further decreased, the centre groove reaches the full depth of the resist film, thus splitting the feature completely and lowering the CD dramatically. This splitting threshold is correlated with exposure dose, as illustrated with vertical lines in Figure 3, despite being difficult to measure accurately due to the discrete nature of mask pattern widths.

It appears that the splitting phenomenon of resist patterns depends both on a target width and DUV exposure dose. Therefore, it can be controlled and used to form different types of Si nanostructures after etching of the 70-nm-thin active Si film, as shown in Figure 4. Whole patterns result in Si nanoribbons of rectangular cross-section with an aspect ratio of about 20:1, or quasi-planar structures. Split patterns result in two parallel nanowires of rectangular section, each with a 2:1 to 6:1 aspect ratio.

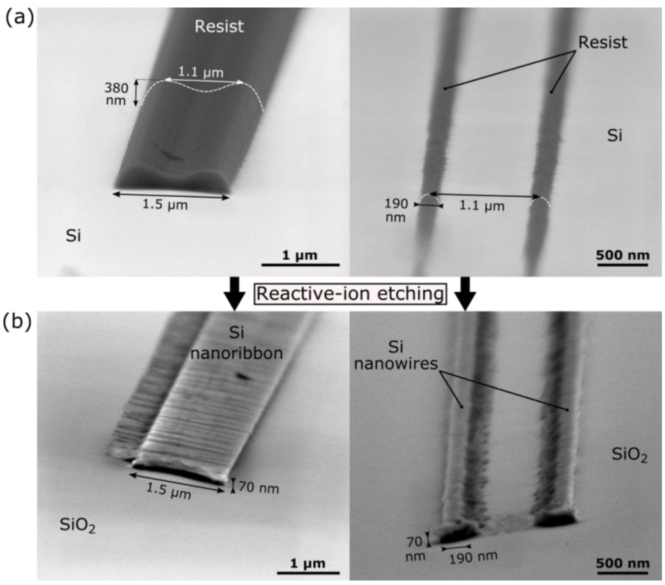

Figure 4. (a) Side-view SEM images of resist features resulting from 1.3 µm (left) and 0.8 µm (right) mask patterns and the same exposure dose of 4 mJ.cm^{-2}. (b) SEM images of the resulting Si features after dry etching by SF_6 RIE and before plasma cleaning.

However, as mentioned previously, it was observed that a single mask pattern and exposure dose can result in different levels of splitting. This is probably caused by non-uniformities in the resist film thickness after spin-coating, which might be significant due to the small size (2x2 cm) and square shape of the SOI samples. The sample size for the lithography was limited to 2x2 cm dies due to process constraints further in the flow. A statistical study was conducted to evaluate the distribution of split and whole Si patterns for three main target widths, at a fixed exposure dose of 4 mJ.cm^{-2}. Figure 5 shows typical nano-ribbon and parallel nanowire structures formed from identical 0.8 µm Cr lines, as well as an intermediary, "discontinuous" state. Thinner mask patterns may also not be resolved at all in certain occurrences.

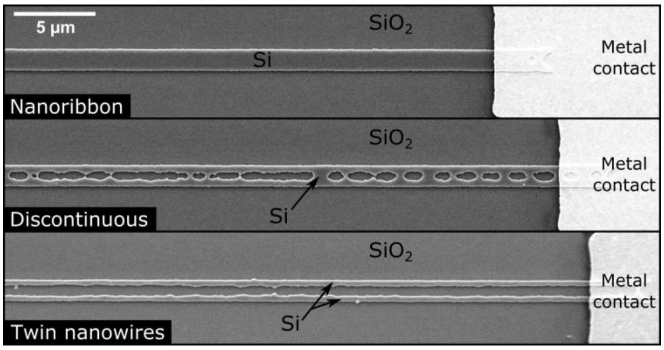

Figure 5. Top-view SEM images of the different types of Si nanostructures resulting from DUV lithography with identical 0.8 µm wide linear patterns on a single SOI substrate, followed by reactive ion etching. Si features are colourized in blue and coated with metal on the right end.

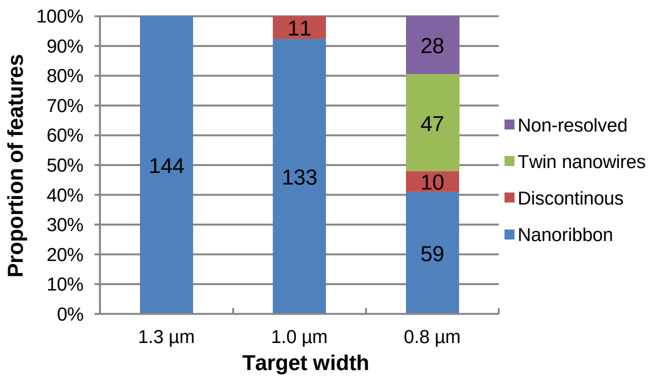

Figure 6.A statistical distribution of the different types of Si nanostructures, based on 144 features obtained on a single wafer from 3 target widths after photolithography (UV5 resist with 4 mJ.cm^{-2} exposure dose)and etching of the topmost layer.

The proportion of each type of structure obtained from a single SOI substrate and single exposure was evaluated qualitatively, based on 144 patterns from each of the three Cr line widths, and the results are reported in Figure 6. It appears that 7 to 8 % of patterns with target width 0.8 or 1.0 µm are partially split (discontinuous), while none of the patterns with target width 1.3 µm display any discontinuity. Among 0.8 µm patterns, 19 % are not resolved at all which means the resist was completely washed away on that spot. The remaining 0.8 µm patterns are composed of 41 % nanoribbons and 33 % nanowires. The observed differences for a single target width are attributable to a thinner local resist film and divergence of the near-field light beam. There should be a continuous distribution of resist thickness across these patterns, affecting the depth of the groove and thus the splitting condition. This is consistent with observations on process variations: it was observed that by increasing or decreasing the development time, the proportion of unresolved or nanoribbon patterns would increase respectively, but the proportion of intermediary states (discontinuous and twin nanowires) would remain the same. However, further accurate measurements of the resist thickness would be required to confirm this hypothesis.

Based on all these results, it appears that an optimal exposure dose can be determined to produce Si nanoribbons and nanowires from a single SOI substrate and using a single photolithography and etching process. With our process parameters, this dose was fixed at around 4 $mJ.cm^{-2}$. It appears that the process window for obtaining twin nanowires reliably is very narrow. The conventional lithography system used for this study was limited by a fixed power density of 4 $mW.cm^{-2}$, and focus bias could not be tuned. This optimized process enables to virtually achieve a critical dimension of about 150 nm, which is lower than the working wavelength of 248 nm, without the need for expensive e-beam lithography and only using a standard chrome/quartz photomask of CD 0.8 µm. The drawback of this method is a lack of control over the splitting and lack of reproducibility regarding the morphology of resulting nanostructures, especially the irregular width of parallel nanowires.

4. Discussion

In this study, process conditions were determined by adjusting mainly exposure time. This parameter affects the effective development threshold of the photoresist, whereas parameters that affect light intensity contrast – such as the initial resist thickness, top Si thickness and buried oxide thickness – were fixed. Indeed, identical samples cut from a single SOI wafer were used throughout the experiments and pre-exposure parameters for PR were mostly unchanged to ensure reproducibility of the measurements and compatibility with standard Si processes on the photolithography line. Also, the research facilities used in this study did not allow full tuning of the process window. Variations of resolution with Cr pattern width were also studied and results indicate that split-patterning may happen similarly with wider Cr lines as the exposure dose increases. This method enables to fabricate split nanolines efficiently by tuning the exposure dose based on target CD.

Experiments were conducted to identify the cause of pattern splitting and attempt to overcome it. Optical properties of SOI substrates differ drastically from bulk Si wafers due to the stacking of thin films having different refractive indexes (Figure 7). Specifically, SOI surfaces are much more reflective than Si. While substrates with high UV reflectivity increase the effective dose that is absorbed by the PR, interference of incident and reflected light also decreases light intensity over the substrate. It is possible to lower the reflectivity at the resist/substrate interface by depositing a bottom anti-reflective coating (BARC) before coating the substrates with PR. BARCs absorb light and minimize substrate reflectivity by creating destructive interference between incident and reflected light. To evaluate the effect of substrate reflectivity on the splitting of resist features, we compared the previous results with samples treated with BARC. SOI substrates were spin-coated with a DUV30 BARC (Brewer Science) at 3000 rpm for 45 s to form a 50 nm thin layer, which is the optimal thickness to negate the reflectivity. BARC was baked for 45 s at 180 °C to be stabilized before the PR was deposited. Positive PR was deposited, exposed and developed following the standard process described previously. Then, BARC and active Si layers were etched using SF_6 RIE with an observed etch rate ratio of 14:1. Visual inspection through optical microscopy revealed similar irregular resist profiles to the ones formed without BARC. It appears that the base substrate reflectivity might not be the main cause of pattern splitting, but rather the inhomogeneous distribution of light intensity, and the interference of laterally reflected light due to the photomask being mostly clear.

Irregular resist profiles can be caused by low uniformity of the film thickness, which is negatively affected in the case of spin-coating on small and/or non-circular substrates. On the SOI dies that were used in this study, we noticed that a resist edge bead is formed during spin-coating and is particularly abrupt in the angles. This artefact can induce an air gap between the resist film and the photomask, despite the vacuum contact mode, thus lowering the effective resolution depending on the position along the substrate's surface. To assess the influence on resist features, edge bead removal (EBD) was attempted by locally dissolving the over thickness around the edges of the SOI dies after spin-coating.

However, microscopy observations revealed that EBD had no positive effect on the resolution of resist patterns. Similarly, PR was spin-coated at a higher rotation speed to lower the height of edge beads, with no effect on resist profile either. Therefore, uniformity of resist thickness does not seem to be a predominant cause of pattern splitting.

The most probable cause of the observed resist profile is the diffraction of DUV light by chrome patterns under a critical width. According to the Huygens-Fresnel principle, obstruction of the beam by the metal edges of chrome patterns could generate new wavefronts, and constructive interference between the first diffraction orders could generate the ridged image in the resist profile. Moreover, even with perfect contact, lateral distribution of light intensity on the resist surface is inhomogeneous because the finite air gap thickness creates a diffraction pattern under the mask. However, the air gap could not be measured and further studied in these experiments.

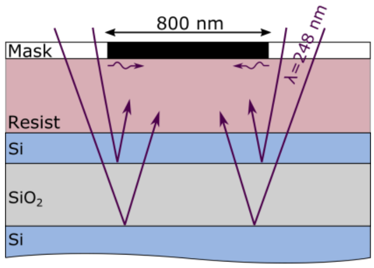

Figure 7. Simplified schematic cross-section view of the reflected and diffused light supposedly contributing to constructive interference under the mask patterns.

The numerical simulation offers more flexibility than experimental work, in the study of the fabrication parameters such as the air gap and photoresist thickness. It also improves the understanding of the optical theory behind the generated irregular resist profiles. Thus, an extensive numerical two-dimensional DUV lithography process simulation was conducted by using ATHENA's Optolith to supplement the real experiments done in the laboratory. Optolith tool performs all key steps of the optical lithography processing including calculation of the 2D aerial imaging of the mask patterns, simulation of the light intensity propagation through photoresist and calculation of the exposure distribution, post-exposure bake and calculation removal of the exposed photoresist[16].To determine the final simulation profiles of the photoresist, the aerial image, exposure and development were simulated. Initially, the elementary process parameters and conditions, counting mask data, UV light intensity, the gap between photoresist and mask, exposure time, photoresist thickness, development time, were described as the basic operations to create the input file of the simulation[17]. Afterwards, the aerial image simulation is conducted to show the illumination of the mask from the top by the incident DUV light source. All along with the exposure simulation, the DUV light propagation is simulated. Following, the post-exposure bake (PEB) and the development rate distribution in the photoresist is obtained. Afterwards, the aerial image is transferred into the resist. Figure 8 shows the cross-section of the 2D light intensity distribution under the line-shaped mask patterns of different widths inside the photoresist (named bulk image) for mask patterns of different widths d=0.8 µm, 1 µm, 1.3 µm, 2 µm respectively.

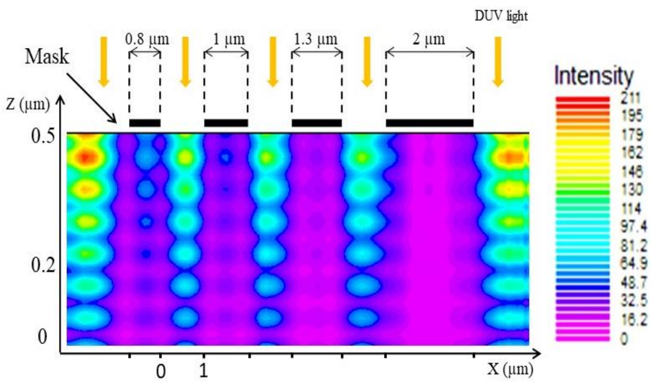

Figure 8. Bulk image simulation showing the mask patterns and the light intensity distribution in the photoresist below the photomask under d=0.8 µm, 1µm, 1.3 µm and 2 µm, d is the width of the line pattern. Distances between mask patterns are equally respected.

The light at the bottom of the photoresist (the exposed photoresist, parts not covered with the mask patterns) is gradually scattering owing to the light diffraction effect. The middle part of the photoresist regions covered by the chrome mask patterns show also incident light distribution that also gradually scatter due to the light diffraction. The amount of light diffraction at the photoresist region under opaque mask features is directly proportional to the width size of the mask patterns. Following, the development of the exposed photoresist is simulated and figure 9 shows the resulting photoresist profiles.

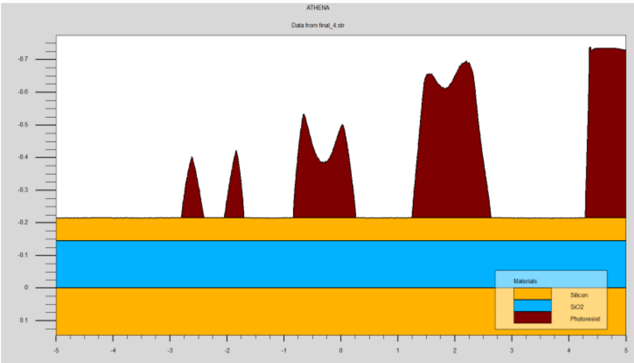

Figure 9. 2D simulation of the resulting photoresist profile after insolation and then development for different mask features widths d=0.8 µm, 0.1 µm, 1.3 µm, 2 µm (from left to right)

The resulting profiles show a complete splitting of the photoresist corresponding to the 0.8 µm mask patterns and this is completely in agreement with the experimental results shown in figure 4. The photoresist profiles after development for larger mask patterns shows also an approximate shape of splitting (not completed) but with a double sine wave shape. The resulting profiles of the photoresist reflect the behaviour of the light distribution at the photoresist according to the bulk image. Thus, the light intensity when reaches a threshold value, the photoresist will get the appropriate energy to release the reaction and to turn liquid, otherwise, it will not be removed in the development step. Thus, the thickness of the photoresist is a key parameter to generate the splitting behaviour of the photoresist as the rate penetration of the light intensity should cross the total depth of the photoresist layer.

The near field or Fresnel diffraction regime can be applied in the case of operating proximity and contact exposure systems which is the case of our experimental and simulation process. So the light passing through the mask results in a diffraction pattern that directly pings on the resist surface as there is no lens between the mask and the resist on the wafer. This means that the created aerial image depends on the near field diffraction pattern. So for the moment if we consider a line-shaped mask pattern of a small width about the same size as the wavelength, and according to the Huygens's principle applied to a straight wavefront (DUV light) striking an obstacle (mask pattern), the edges of the wavefront bend after passing around the mask pattern and this process is called diffraction [18]. For small mask patterns, the amount of bending is more extreme, logical with the fact that wave characteristics are most noticeable for interactions with objects about the same size as the wavelength. This is noticeable from the gradual intensity rises near the edges of the mask features (obstacle). Adding to that and because of the diffractions effects, the light binds away from the mask features resulting in the resist exposure at the region underneath the opaque mask patterns. Considering now that a small gap is separating the mask and the photoresist on the wafer. The diffracted waves (binding) are assumed to be incident on the mask aperture and as the gap increases the destructive and constructive interferences between the Huygens wavelets emanating around the mask feature arise resulting in the apparition of the intensity distribution within the middle part of the non-exposed region. Simulation results of the same process but at gap value of zero show no splitting behaviour of the photoresist. For a targeted and reproducible process, additional experimental work (according to the simulation results) on the air gap fluctuation and resist thickness can be conducted to increase the yield of split nanolines.

5. Conclusion

In this paper, we report a fabrication process of Si nanostructures with sub-wavelength critical dimension involving deep-UV wave interferences lithography. Lithographic process parameters were optimized to take advantage of irregular resist profiles obtained on SOI substrates due to in-plane interference. We show that optimal exposure dose, exact gap value, photoresist thickness and specific mask patterns size can be determined to elaborate resist features with different morphologies, resulting in Si linear structures of nanoribbon or nanowire type. Using these optimal exposure parameters, mark patterns of width 0.8 µm can be used to generate nanowires down to 150 nm wide, along with high aspect-ratio nanoribbons, from a single SOI substrate. The method presented here enables fast and cost-effective pattern transfer at a potentially large scale, compared to e-beam lithography which has a similar resolution, at the expense of reproducibility and fine CD control. This process can be combined with the subsequent trimming to reduce the size of the Si NWs, e.g. through thermal oxidation cycles, and enables the parallel fabrication of NR FETs and twin NW FETs from SOI substrates.

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