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1 Optimizing Interferences of DUV Lithography on 2 SOI Substrates for the Rapid Fabrication of 3 Subwavelength Features

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13 Abstract

14 Scalable fabrication of Si nanowires with a critical dimension of about 100 nm is essential to
15 a variety of applications. Current techniques used to reach these dimensions often involve
16 e-beam lithography or DUV lithography combined with resolution enhancement techniques.
17 In this study, we report the fabrication of <150nm Si nanowires from SOI substrates using
18 DUV lithography ($\lambda = 248$ nm) by adjusting the exposure dose. Irregular resist profiles
19 generated by in-plane interference under masking patterns of width 800 nm were optimized to
20 split the resulting features into twin Si nanowires. However, masking patterns of micrometre
21 size or more on the same photomask does not generate split features. The resulting resist
22 profiles are verified by optical lithography computer simulation based on Huygens-Fresnel
23 diffraction theory. Photolithography simulation results validate that the key factors in the
24 fabrication of subwavelength nanostructures are the air gap value and the photoresist
25 thickness. This enables the parallel top-down fabrication of Si nanowires and nanoribbons in
26 a single DUV lithography step as a rapid and inexpensive alternative to conventional e-beam
27 techniques.

28 Keywords: photolithography, deep ultraviolet, silicon on insulator, nanowire

29

30 1. Introduction

31 Si nanowires (NW) are used in a variety of
32 applications, including the recent research on field-effect
33 transistor (FET) sensors, in particular on biosensors [1]–
34 [4], due to their high surface-to-volume ratio and electron
35 mobility. Alternative structures like Si nanoribbons (NR)
36 can efficiently replace NWs in such sensing applications,
37 where lateral critical dimension (CD) is not a crucial
38 parameter [5]–[8]. Top-down fabricated Si NWs are
39 generally preferred over bottom-up NWs because of their
40 compatibility with CMOS technology. However,

41 achieving feature sizes of 100 nm and below is still
42 challenging without industry-grade equipment, and
43 generally requires costly e-beam lithography processes or
44 the combination of deep-UV (DUV) lithography with size
45 reduction methods. Methods for reducing the size of Si
46 NWs include the use of spacers and sacrificial layers [9],
47 mesa isolation techniques, controlled anisotropic etching
48 [1], [10], resist trimming, or thinning down Si features
49 through cycles of thermal oxidation and selective oxide
50 etch. These methods extend the resolution limits of
51 lithography and can result in feature sizes down to about
52 10 nm, potentially. However, some of these methods are
53 not compatible with silicon-on-insulator (SOI) substrates,

1 which are playing a growing role in advanced CMOS
2 processes.

3
4 Here, we present an alternative fabrication method of
5 Si NWs from SOI substrates using DUV lithography. By
6 taking advantage of in-plane interference and adjusting
7 exposure parameters, it is possible to generate ridged
8 resist features resulting in isolated twin NWs and to reach
9 sub-wavelength CD. Interference between the incident
10 wave and the reflected wave due to substrate reflectivity
11 can generate vertical standing-wave roughness on resist
12 sidewalls [11] and is generally suppressed by adding a
13 bottom anti-reflective coating (BARC) to the resist stack
14 [12]. In-plane interference is used in laser interference
15 lithography (LIL) as a maskless technique to generate
16 periodic nanodot or nanowire patterns on a large scale
17 [13]–[15]. In this study, isolated horizontal interference
18 patterns were observed, inducing wave variations in the
19 resist profile, and were exploited to split Si features into
20 twin NWs. Nanowires with a CD down to 120 nm were
21 successfully fabricated from 800 nm mask pattern in a
22 single step, without any thinning process, by optimizing
23 the exposure dose. This method allows fast prototyping
24 and scalable fabrication of NWs and NRs without the
25 need for expensive and time-consuming e-beam
26 lithography. Extensive optical lithography numerical
27 simulation is conducted by ATHENA's Optolith (Silvaco)
28 in which the experimental process flow of fabrication is
29 respected. The simulation results confirm that the air gap
30 value (between the mask patterns and the photoresist
31 surface), photoresist thickness and the mask patterns
32 width are the key factors allowing the introduction of
33 diffractions in the conventional DUV lithography
34 process.

36 2. Materials and methods

37 SOI substrates with 70-nm-thin single-crystal Si film
38 and 145-nm-thin buried oxide were spin-coated by UV5
39 (Microchemicals) positive photoresist (PR) at 4000 rpm
40 for an expected thickness of about 0.525 μm , and baked
41 for 60 s at 130 $^{\circ}\text{C}$. Substrates were aligned with a
42 quartz/chrome mask holding linear patterns of widths 0.8,
43 1.0 and 1.3 μm using a Süss Microtech MJB4 mask
44 aligner in vacuum contact mode. The samples were
45 exposed for 1 s by a Hg/Xe deep-UV (DUV) source with
46 a nominal power of 4 $\text{mW}\cdot\text{cm}^{-2}$ at wavelength 248 nm.

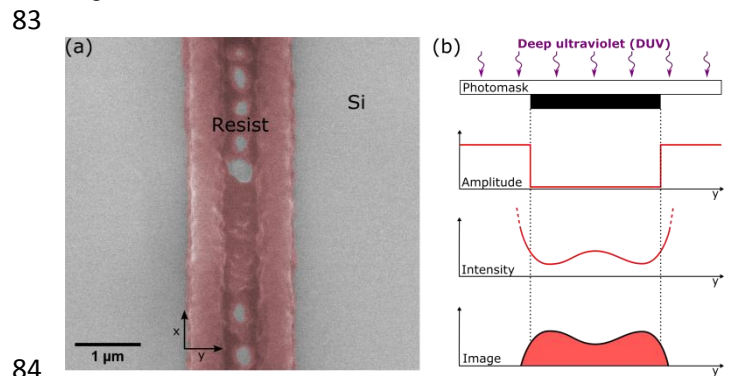
47 For optimization purposes, as will be discussed
48 further, the exposure time ranged from 0.9 to 2.6 s. A
49 post-exposure bake was applied for 90 s at 130 $^{\circ}\text{C}$ before
50 the samples were bathed in AZ326MIF developer and
51 rinsed with DIW. The topmost Si film was etched by SF_6
52 reactive ionic etching (RIE) using a Corial 200 IL RIE,

53 and etch depth was controlled by end-point detection
54 (EPD). Resist stripping was then conducted with AR300-
55 76 remover and the surface was cleaned by oxygen
56 plasma.

57 3. Results

58 Exposure parameters for DUV lithography were
59 initially adapted from standard Si processes to be used on
60 SOI substrates. Conformity of the resulting PR and Si
61 patterns to the target dimensions was controlled on bulk
62 Si substrates using the same parameters. However, on
63 SOI substrates, it is noticeable that resist patterns are not
64 correctly resolved. The overall footprint of the linear
65 patterns is wider than the expected 0.8, 1.0 and 1.3 μm .
66 As shown on Figure 1a and 1b, the resist features have
67 curved lateral walls, inclined with an angle of about 75 $^{\circ}$
68 with the surface, and a ridged cross-section split by a
69 groove in the middle.

70
71 The feature shown in Figure 1a was obtained using
72 UV5 resist and exposing it for 1.3 s, which was the
73 standard for Si. Since it is a positive resist, the middle
74 groove indicates a partially overexposed area centred
75 underneath opaque chrome patterns. The spatial profile of
76 resist features provides information about the actual
77 distribution of light intensity in the resist volume
78 compared to the expected amplitude generated by the
79 masking patterns, as illustrated in Figure 1b. The cross-
80 sectional shape can also be found in the plane of the Si
81 surface, as parabolic lobes are formed instead of right
82 angles.



84
85 **Figure 1.** (a) Top-view SEM images of typical resist features obtained
86 by deep-UV lithography of a linear pattern of 1.3 μm width on 70/145
87 nm SOI substrates. The photoresist is colorized in red. (b) Schematic
88 cross-section view of the light profile under a chrome pattern and the
89 resulting positive PR feature.

90
91 The morphology of resist features was investigated
92 using SEM with variable target width. Figure 2 shows the
93 resist image of crossed linear mask patterns, which range
94 from 0.8 to 2 μm in width. The exposure time was fixed
95 at 2 s to deliver a dose of 8 $\text{mJ}\cdot\text{cm}^{-2}$. SEM images show

1 that the middle groove is almost absent from 2 μm
 2 patterns and becomes deeper and wider as the target
 3 width decreases, until the total splitting of the features
 4 under 1 μm . The peak resist thickness on isolated lines
 5 ranges from 0.5 μm for wide lines down to about 0.1 μm

6 for split nanolines. Regarding the measured width,
 7 patterns of width 1.6 μm and more appear to be
 8 transferred with high fidelity, whereas smaller patterns
 9 generate a footprint of limit width 1.4 μm approximately.

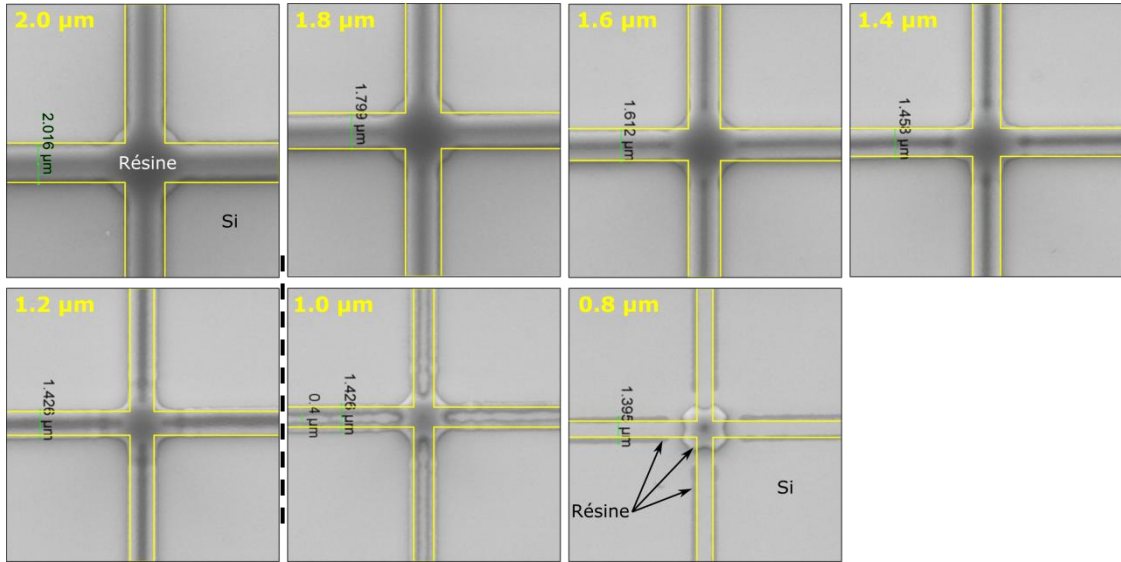


Figure 2. Top-view SEM images of UV5 resist features formed on an SOI substrate from intersecting mask patterns, with a width ranging from 0.8 to 2.0 μm , using DUV lithography (248 nm) at an exposure dose 8 $\text{mJ}\cdot\text{cm}^{-2}$. Target patterns are drawn as yellow frames.

The results presented above indicate that the resist profile varies non-linearly with the Cr mask pattern width at a set exposure dose. In this case, a critical target width between 1.0 and 1.2 μm represents the "splitting threshold" where the centre groove due to induced exposure is deep enough to reach the substrate. This threshold is illustrated as a dashed line in Figure 2.

The influence of exposure dose was also conducted to optimize process parameters. Several samples coated with PR of the same thickness were exposed for 1 to 2.6 s with a surface power density fixed at 4 $\text{mW}\cdot\text{cm}^{-2}$. All other process parameters were identical between the samples and the resulting resist features after development was studied by SEM.

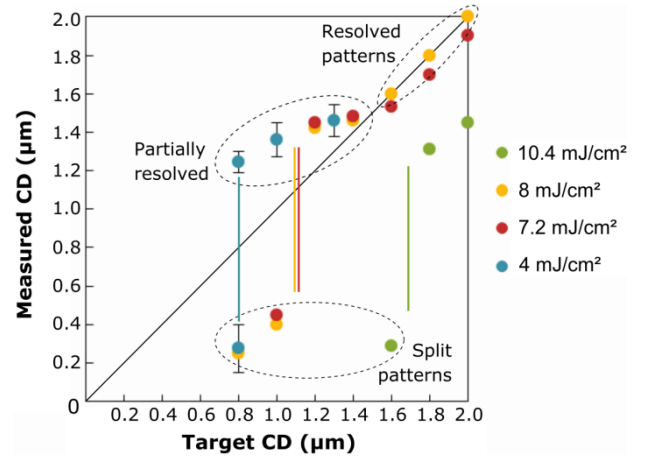


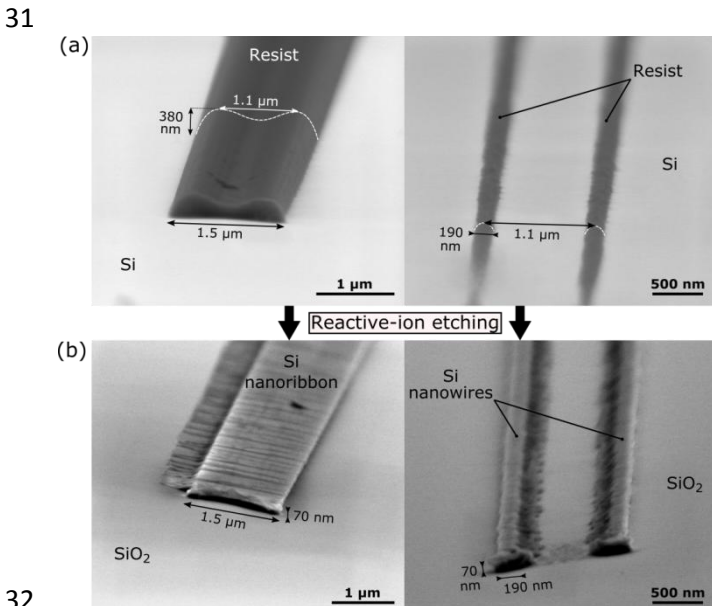
Figure 3. Average measured critical dimension (CD) of resist features as a function of mask target CD for different exposure doses of UV5 resist on SOI. Error bars correspond to the standard deviation, based on the measurements of about 100 nanostructures obtained with the optimal experimental dose.

Figure 3 shows the plot of the average measured critical dimension (CD) as a function of target width, for different exposure doses. A single mask pattern may result in whole resist features or split ones. In this case, the resulting CDs are displayed as two separate populations, as can be seen at $\text{CD}_{\text{target}} = 0.8 \mu\text{m}$ for the sample exposed by 4 $\text{mJ}\cdot\text{cm}^{-2}$.

Results show that the actual resist width varies non-linearly as a function of target width along with the mask

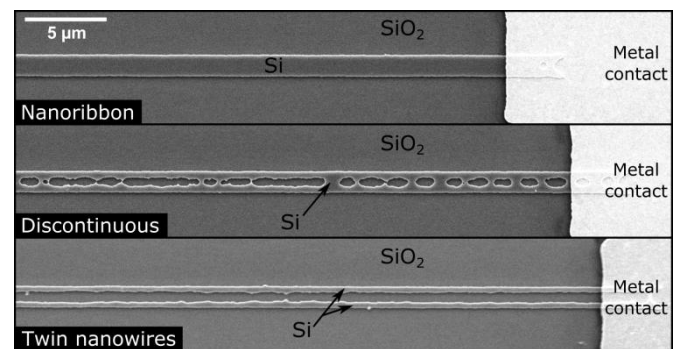
1 patterns' range. Only the largest targets ($CD > 1.5 \mu\text{m}$)
 2 are resolved accurately with a moderate exposure dose of
 3 $7\text{--}8 \text{ mJ}\cdot\text{cm}^{-2}$. With a larger dose, a bigger volume of resist
 4 is made soluble to the developer and thus the patterns are
 5 reasonably narrower. Oppositely, under-exposure results
 6 in wider resist patterns. However, under a critical target
 7 width of about $1.5 \mu\text{m}$, data no longer fits with the
 8 bisector line as the resist features displayed a wider
 9 footprint than expected. These partially resolved features
 10 do result as single lines of resist, but with a linewidth
 11 print bias and a deep central groove which may produce
 12 holes on silicon. When the target width is further
 13 decreased, the centre groove reaches the full depth of the
 14 resist film, thus splitting the feature completely and
 15 lowering the CD dramatically. This splitting threshold is
 16 correlated with exposure dose, as illustrated with vertical
 17 lines in Figure 3, despite being difficult to measure
 18 accurately due to the discrete nature of mask pattern
 19 widths.

20
 21 It appears that the splitting phenomenon of resist
 22 patterns depends both on a target width and DUV
 23 exposure dose. Therefore, it can be controlled and used to
 24 form different types of Si nanostructures after etching of
 25 the 70-nm-thin active Si film, as shown in Figure 4.
 26 Whole patterns result in Si nanoribbons of rectangular
 27 cross-section with an aspect ratio of about 20:1, or quasi-
 28 planar structures. Split patterns result in two parallel
 29 nanowires of rectangular section, each with a 2:1 to 6:1
 30 aspect ratio.

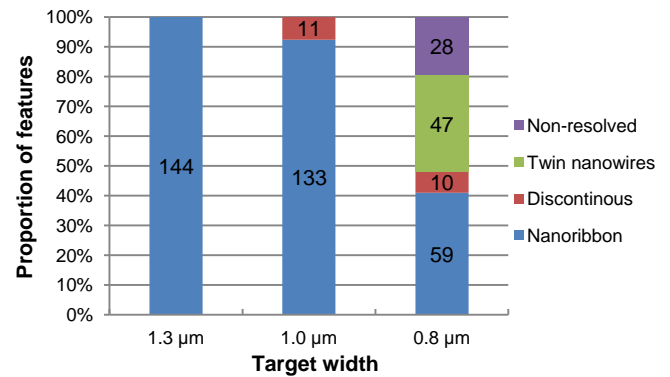


32
 33 **Figure 4.** (a) Side-view SEM images of resist features resulting from
 34 $1.3 \mu\text{m}$ (left) and $0.8 \mu\text{m}$ (right) mask patterns and the same exposure
 35 dose of $4 \text{ mJ}\cdot\text{cm}^{-2}$. (b) SEM images of the resulting Si features after dry
 36 etching by SF_6 RIE and before plasma cleaning.

37 However, as mentioned previously, it was observed
 38 that a single mask pattern and exposure dose can result in
 39 different levels of splitting. This is probably caused by
 40 non-uniformities in the resist film thickness after spin-
 41 coating, which might be significant due to the small size
 42 ($2 \times 2 \text{ cm}$) and square shape of the SOI samples. The
 43 sample size for the lithography was limited to $2 \times 2 \text{ cm}$
 44 dies due to process constraints further in the flow. A
 45 statistical study was conducted to evaluate the
 46 distribution of split and whole Si patterns for three main
 47 target widths, at a fixed exposure dose of $4 \text{ mJ}\cdot\text{cm}^{-2}$.
 48 Figure 5 shows typical nano-ribbon and parallel nanowire
 49 structures formed from identical $0.8 \mu\text{m}$ Cr lines, as well
 50 as an intermediary, "discontinuous" state. Thinner mask
 51 patterns may also not be resolved at all in certain
 52 occurrences.



53
 54 **Figure 5.** Top-view SEM images of the different types of Si
 55 nanostructures resulting from DUV lithography with identical $0.8 \mu\text{m}$
 56 wide linear patterns on a single SOI substrate, followed by reactive ion
 57 etching. Si features are colorized in blue and coated with metal on the
 58 right end.



59
 60 **Figure 6.** A statistical distribution of the different types of Si
 61 nanostructures, based on 144 features obtained on a single wafer from 3
 62 target widths after photolithography (UV5 resist with $4 \text{ mJ}\cdot\text{cm}^{-2}$
 63 exposure dose) and etching of the topmost layer.

64
 65 The proportion of each type of structure obtained from
 66 a single SOI substrate and single exposure was evaluated
 67 qualitatively, based on 144 patterns from each of the
 68 three Cr line widths, and the results are reported in Figure
 69 6. It appears that 7 to 8 % of patterns with target width
 70 0.8 or $1.0 \mu\text{m}$ are partially split (discontinuous), while

1 none of the patterns with target width 1.3 μm display any
2 discontinuity. Among 0.8 μm patterns, 19 % are not
3 resolved at all which means the resist was completely
4 washed away on that spot. The remaining 0.8 μm patterns
5 are composed of 41 % nanoribbons and 33 % nanowires.
6 The observed differences for a single target width are
7 attributable to a thinner local resist film and divergence of
8 the near-field light beam. There should be a continuous
9 distribution of resist thickness across these patterns,
10 affecting the depth of the groove and thus the splitting
11 condition. This is consistent with observations on process
12 variations: it was observed that by increasing or
13 decreasing the development time, the proportion of
14 unresolved or nanoribbon patterns would increase
15 respectively, but the proportion of intermediary states
16 (discontinuous and twin nanowires) would remain the
17 same. However, further accurate measurements of the
18 resist thickness would be required to confirm this
19 hypothesis.

20
21 Based on all these results, it appears that an optimal
22 exposure dose can be determined to produce Si
23 nanoribbons and nanowires from a single SOI substrate
24 and using a single photolithography and etching process.
25 With our process parameters, this dose was fixed at
26 around 4 $\text{mJ}\cdot\text{cm}^{-2}$. It appears that the process window for
27 obtaining twin nanowires reliably is very narrow. The
28 conventional lithography system used for this study was
29 limited by a fixed power density of 4 $\text{mW}\cdot\text{cm}^{-2}$, and focus
30 bias could not be tuned. This optimized process enables
31 to virtually achieve a critical dimension of about 150 nm,
32 which is lower than the working wavelength of 248 nm,
33 without the need for expensive e-beam lithography and
34 only using a standard chrome/quartz photomask of CD
35 0.8 μm . The drawback of this method is a lack of control
36 over the splitting and lack of reproducibility regarding the
37 morphology of resulting nanostructures, especially the
38 irregular width of parallel nanowires.

39 4. Discussion

40 In this study, process conditions were determined by
41 adjusting mainly exposure time. This parameter affects
42 the effective development threshold of the photoresist,
43 whereas parameters that affect light intensity contrast –
44 such as the initial resist thickness, top Si thickness and
45 buried oxide thickness – were fixed. Indeed, identical
46 samples cut from a single SOI wafer were used
47 throughout the experiments and pre-exposure parameters
48 for PR were mostly unchanged to ensure reproducibility
49 of the measurements and compatibility with standard Si
50 processes on the photolithography line. Also, the research
51 facilities used in this study did not allow full tuning of the
52 process window. Variations of resolution with Cr pattern

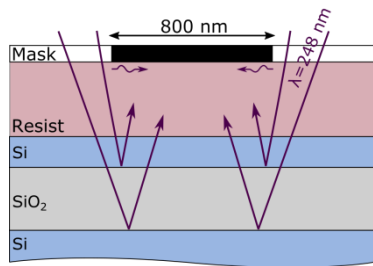
53 width were also studied and results indicate that split-
54 patterning may happen similarly with wider Cr lines as
55 the exposure dose increases. This method enables to
56 fabricate split nanolines efficiently by tuning the
57 exposure dose based on target CD.

58
59 Experiments were conducted to identify the cause of
60 pattern splitting and attempt to overcome it. Optical
61 properties of SOI substrates differ drastically from bulk
62 Si wafers due to the stacking of thin films having
63 different refractive indexes (Figure 7). Specifically, SOI
64 surfaces are much more reflective than Si. While
65 substrates with high UV reflectivity increase the effective
66 dose that is absorbed by the PR, interference of incident
67 and reflected light also decreases light intensity over the
68 substrate. It is possible to lower the reflectivity at the
69 resist/substrate interface by depositing a bottom anti-
70 reflective coating (BARC) before coating the substrates
71 with PR. BARCs absorb light and minimize substrate
72 reflectivity by creating destructive interference between
73 incident and reflected light. To evaluate the effect of
74 substrate reflectivity on the splitting of resist features, we
75 compared the previous results with samples treated with
76 BARC. SOI substrates were spin-coated with a DUV30
77 BARC (Brewer Science) at 3000 rpm for 45 s to form a
78 50 nm thin layer, which is the optimal thickness to negate
79 the reflectivity. BARC was baked for 45 s at 180 °C to be
80 stabilized before the PR was deposited. Positive PR was
81 deposited, exposed and developed following the standard
82 process described previously. Then, BARC and active Si
83 layers were etched using SF_6 RIE with an observed etch
84 rate ratio of 14:1. Visual inspection through optical
85 microscopy revealed similar irregular resist profiles to the
86 ones formed without BARC. It appears that the base
87 substrate reflectivity might not be the main cause of
88 pattern splitting, but rather the inhomogeneous
89 distribution of light intensity, and the interference of
90 laterally reflected light due to the photomask being
91 mostly clear.

92
93 Irregular resist profiles can be caused by low
94 uniformity of the film thickness, which is negatively
95 affected in the case of spin-coating on small and/or non-
96 circular substrates. On the SOI dies that were used in this
97 study, we noticed that a resist edge bead is formed during
98 spin-coating and is particularly abrupt in the angles. This
99 artefact can induce an air gap between the resist film and
100 the photomask, despite the vacuum contact mode, thus
101 lowering the effective resolution depending on the
102 position along the substrate's surface. To assess the
103 influence on resist features, edge bead removal (EBD)
104 was attempted by locally dissolving the over thickness
105 around the edges of the SOI dies after spin-coating.

1 However, microscopy observations revealed that EBD
 2 had no positive effect on the resolution of resist patterns.
 3 Similarly, PR was spin-coated at a higher rotation speed
 4 to lower the height of edge beads, with no effect on resist
 5 profile either. Therefore, uniformity of resist thickness
 6 does not seem to be a predominant cause of pattern
 7 splitting.

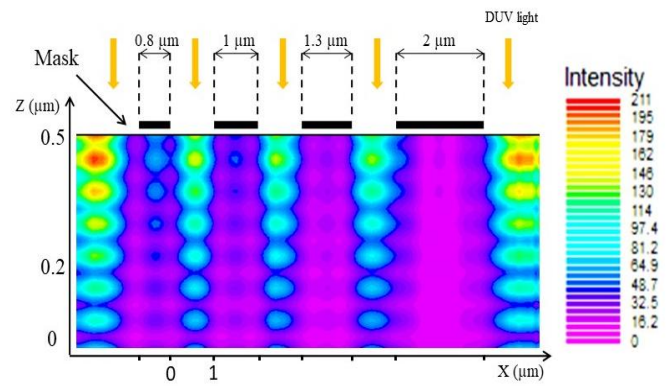
8
 9 The most probable cause of the observed resist profile
 10 is the diffraction of DUV light by chrome patterns under
 11 a critical width. According to the Huygens-Fresnel
 12 principle, obstruction of the beam by the metal edges of
 13 chrome patterns could generate new wavefronts, and
 14 constructive interference between the first diffraction
 15 orders could generate the ridged image in the resist
 16 profile. Moreover, even with perfect contact, lateral
 17 distribution of light intensity on the resist surface is
 18 inhomogeneous because the finite air gap thickness
 19 creates a diffraction pattern under the mask. However, the
 20 air gap could not be measured and further studied in these
 21 experiments.



23
 24 **Figure 7.** Simplified schematic cross-section view of the reflected and
 25 diffused light supposedly contributing to constructive interference under
 26 the mask patterns.

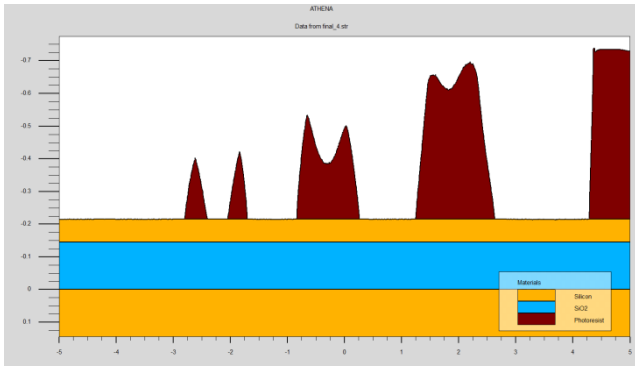
27
 28 The numerical simulation offers more flexibility than
 29 experimental work, in the study of the fabrication
 30 parameters such as the air gap and photoresist thickness.
 31 It also improves the understanding of the optical theory
 32 behind the generated irregular resist profiles. Thus, an
 33 extensive numerical two-dimensional DUV lithography
 34 process simulation was conducted by using ATHENA's
 35 Optolith to supplement the real experiments done in the
 36 laboratory. Optolith tool performs all key steps of the
 37 optical lithography processing including calculation of
 38 the 2D aerial imaging of the mask patterns, simulation of
 39 the light intensity propagation through photoresist and
 40 calculation of the exposure distribution, post-exposure
 41 bake and calculation removal of the exposed
 42 photoresist[16]. To determine the final simulation profiles
 43 of the photoresist, the aerial image, exposure and
 44 development were simulated. Initially, the elementary
 45 process parameters and conditions, counting mask data,
 46 UV light intensity, the gap between photoresist and mask,

47 exposure time, photoresist thickness, development time,
 48 were described as the basic operations to create the input
 49 file of the simulation[17]. Afterwards, the aerial image
 50 simulation is conducted to show the illumination of the
 51 mask from the top by the incident DUV light source. All
 52 along with the exposure simulation, the DUV light
 53 propagation is simulated. Following, the post-exposure
 54 bake (PEB) and the development rate distribution in the
 55 photoresist is obtained. Afterwards, the aerial image is
 56 transferred into the resist. Figure 8 shows the cross-
 57 section of the 2D light intensity distribution under the
 58 line-shaped mask patterns of different widths inside the
 59 photoresist (named bulk image) for mask patterns of
 60 different widths $d=0.8 \mu\text{m}$, $1 \mu\text{m}$, $1.3 \mu\text{m}$, $2 \mu\text{m}$
 61 respectively.



62
 63 **Figure 8.** Bulk image simulation showing the mask patterns and the
 64 light intensity distribution in the photoresist below the photomask under
 65 $d=0.8 \mu\text{m}$, $1 \mu\text{m}$, $1.3 \mu\text{m}$ and $2 \mu\text{m}$, d is the width of the line pattern.
 66 Distances between mask patterns are equally respected.

67 The light at the bottom of the photoresist (the exposed
 68 photoresist, parts not covered with the mask patterns) is
 69 gradually scattering owing to the light diffraction effect.
 70 The middle part of the photoresist regions covered by the
 71 chrome mask patterns show also incident light
 72 distribution that also gradually scatter due to the light
 73 diffraction. The amount of light diffraction at the
 74 photoresist region under opaque mask features is directly
 75 proportional to the width size of the mask patterns.
 76 Following, the development of the exposed photoresist is
 77 simulated and figure 9 shows the resulting photoresist
 78 profiles.



1
2 **Figure 9.** 2D simulation of the resulting photoresist profile after
3 insolation and then development for different mask features widths
4 $d=0.8 \mu\text{m}$, $0.1 \mu\text{m}$, $1.3 \mu\text{m}$, $2 \mu\text{m}$ (from left to right)

5 The resulting profiles show a complete splitting of the
6 photoresist corresponding to the $0.8 \mu\text{m}$ mask patterns
7 and this is completely in agreement with the experimental
8 results shown in figure 4. The photoresist profiles after
9 development for larger mask patterns shows also an
10 approximate shape of splitting (not completed) but with a
11 double sine wave shape. The resulting profiles of the
12 photoresist reflect the behaviour of the light distribution
13 at the photoresist according to the bulk image. Thus, the
14 light intensity when reaches a threshold value, the
15 photoresist will get the appropriate energy to release the
16 reaction and to turn liquid, otherwise, it will not be
17 removed in the development step. Thus, the thickness of
18 the photoresist is a key parameter to generate the splitting
19 behaviour of the photoresist as the rate penetration of the
20 light intensity should cross the total depth of the
21 photoresist layer.

22 The near field or Fresnel diffraction regime can be
23 applied in the case of operating proximity and contact
24 exposure systems which is the case of our experimental
25 and simulation process. So the light passing through the
26 mask results in a diffraction pattern that directly pings on
27 the resist surface as there is no lens between the mask and
28 the resist on the wafer. This means that the created aerial
29 image depends on the near field diffraction pattern. So for
30 the moment if we consider a line-shaped mask pattern of
31 a small width about the same size as the wavelength, and
32 according to the Huygens's principle applied to a straight
33 wavefront (DUV light) striking an obstacle (mask
34 pattern), the edges of the wavefront bend after passing
35 around the mask pattern and this process is called
36 diffraction [18]. For small mask patterns, the amount of
37 bending is more extreme, logical with the fact that wave
38 characteristics are most noticeable for interactions with
39 objects about the same size as the wavelength. This is

40 noticeable from the gradual intensity rises near the edges
41 of the mask features (obstacle). Adding to that and
42 because of the diffractions effects, the light binds away
43 from the mask features resulting in the resist exposure at
44 the region underneath the opaque mask patterns.
45 Considering now that a small gap is separating the mask
46 and the photoresist on the wafer. The diffracted waves
47 (binding) are assumed to be incident on the mask aperture
48 and as the gap increases the destructive and constructive
49 interferences between the Huygens wavelets emanating
50 around the mask feature arise resulting in the apparition
51 of the intensity distribution within the middle part of the
52 non-exposed region. Simulation results of the same
53 process but at gap value of zero show no splitting
54 behaviour of the photoresist. For a targeted and
55 reproducible process, additional experimental work
56 (according to the simulation results) on the air gap
57 fluctuation and resist thickness can be conducted to
58 increase the yield of split nanolines.

59 5. Conclusion

60 In this paper, we report a fabrication process of Si
61 nanostructures with sub-wavelength critical dimension
62 involving deep-UV wave interferences lithography.
63 Lithographic process parameters were optimized to take
64 advantage of irregular resist profiles obtained on SOI
65 substrates due to in-plane interference. We show that
66 optimal exposure dose, exact gap value, photoresist
67 thickness and specific mask patterns size can be
68 determined to elaborate resist features with different
69 morphologies, resulting in Si linear structures of
70 nanoribbon or nanowire type. Using these optimal
71 exposure parameters, mark patterns of width $0.8 \mu\text{m}$ can
72 be used to generate nanowires down to 150 nm wide,
73 along with high aspect-ratio nanoribbons, from a single
74 SOI substrate. The method presented here enables fast
75 and cost-effective pattern transfer at a potentially large
76 scale, compared to e-beam lithography which has a
77 similar resolution, at the expense of reproducibility and
78 fine CD control. This process can be combined with the
79 subsequent trimming to reduce the size of the Si NWs,
80 e.g. through thermal oxidation cycles, and enables the
81 parallel fabrication of NR FETs and twin NW FETs from
82 SOI substrates.

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