# Open-air, low-temperature deposition of phase pure Cu 2 O thin films as efficient hole-transporting layers for silicon heterojunction solar cells

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COMMUNICATION

# Open-Air, Low-Temperature Deposition of Phase Pure $Cu_2O$ Thin Films as Efficient Hole-Transporting Layers for Silicon Heterojunction Solar Cells

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**Recent research focuses on finding alternative materials and fabrication techniques to replace traditional (p) and (n) doped hydrogenated amorphous silicon (a-Si:H) to reduce cost and boost the efficiency of Silicon Heterojunction (SHJ) solar cells. In this work, low-cost p-type $Cu_2O$ thin films have been investigated and integrated as a hole-transporting layer (HTL) in SHJ solar cells, using Atmospheric-Pressure Spatial Atomic Layer Deposition (AP-SALD), an open-air, scalable ALD approach. Phase pure $Cu_2O$ thin films have been deposited at temperatures below the degradation limit of the SHJ, thus maintaining the passivation effect of the a-Si:H layer. The effect of deposition temperatures and HTL thicknesses on the performance of the devices has been evaluated. The fabricated $Cu_2O$ HTL-based SHJ cells, having an area of 9 $cm^2$, reach a power conversion efficiency (PCE) of 13.7%, which is the highest reported efficiency for silicon-based solar cells incorporating a $Cu_2O$ HTL.**

SHJ solar cells combining thin hydrogenated amorphous silicon (a-Si:H) layers with a crystalline silicon (c-Si) absorber are a mature technology that has demonstrated record efficiencies above 25% for large-area devices (~180 $cm^2$), both using the *interdigitated back contact* (IBC) or *both sides contacted* (BSC) architectures.[1–5] The use of a-Si:H layers between the crystalline silicon core and the metal contact promotes a drastic reduction of recombination at the contacts, yielding an increase in the open-circuit voltage.[3,6] The doped thin a-Si:H layers act both as a passivation film on the dangling bonds of the crystalline silicon wafer and as a selective contact. This is mainly attributed to the high hydrogen content and ability to promote doping of these films, together with adequate interface band offsets.[5,7,8] Such passivation effect allows to use thinner c-Si wafers, and thus, this technology represents a promising alternative to the current c-Si technology.[9]

Due to their wider bandgap ( ~1.7 eV) with respect to crystalline silicon, a-Si:H films offer higher transparency, thus facilitating the transmission of photons to the bulk absorber.[10–12] Nevertheless, the transparency of these films is still not enough to avoid parasitic absorption at the front side of the device.[13–15] Another major drawback of the a-Si:H layers is their low conductivity, which therefore increases the series resistance within the device.[16,17] As an alternative, several works focus on the development of nano-crystalline layers (nc-$SiO_x$:H) to substitute the a-Si:H layer, to improve both the conductivity and the transparency of this active window layer.[18–21]

In a different approach, several groups have proposed to replace the a-Si:H films by oxides or alkaline metals,[7,22–24] targeting ultra-low surface recombination velocities, high transparency, excellent carrier selectivity and low resistivity values.[22] Among the different oxides, $Cu_2O$ is a promising semi-transparent p-type HTL thanks to the high abundance of Cu, a work function of 5 eV (close to ~5.2 eV of a-Si:H(p) ), and a wide optical bandgap of approximately 2.1 eV.[25] As a result, $Cu_2O$ has been explored as a component in numerous optoelectronic applications, such as photovoltaics,[26–28] water splitting,[29,30] and photodetectors.[31–33]

The integration of $Cu_2O$ in emerging and industrial-scale solar cell technologies has shown strong interest in recent years:[34] it has been integrated into hybrid perovskite solar cells as a HTL and buffer layer, contributing both to the enhancement of the power conversion efficiency and the stability of the perovskite films.[35–37] In organic solar devices, $Cu_2O$ has demonstrated an improvement in the power conversion efficiency compared to conventional PEDOT:PSS HTL.[38] $Cu_2O$ is also being heavily explored as potential component in Si based PV technologies. Undoped and doped sputtered $Cu_2O$ has been explored for the first time as a hole selective contact in c-Si solar cells.[39] The maximum reached power conversion efficiency reached so far for Si based solar cells is 9.54%, incorporating a solution-processed $Cu_2O$ layer and after introducing $MoO_x$ antireflective coating.[40]

$Cu_2O$ is also potential candidate to replace the a-Si:H(p) layer in SHJ devices due to its high conductivity, matched energy level, and high mobility value.[34,41] But $Cu_2O$ HTLs developed so far in the literature are mostly obtained with growth techniques

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that require either high thermal budgets (>350 °C) or involving several steps. These growth conditions are incompatible with SHJ cells, which require low-temperature processing to preserve the passivation conferred by the a-Si:H. Apart from being able to deposit the $Cu_2O$ layers at maximum temperatures around 200 °C, their implementation in SHJ cells also requires low-cost and scalable processing while retaining good transport properties and high growth rate. Atmospheric Pressure - Spatial Atomic Layer Deposition (AP-SALD) represents an appealing option since it allows the deposition of high-quality thin films at low temperatures and high throughout,[42] even when processing at atmospheric pressure.[43] AP-SALD has indeed already been widely applied to new generation photovoltaic technologies,[44] among others.[45–47] In particular, $Cu_2O$ thin films deposited by SALD have been extensively studied in terms of structural, optical, and electrical properties previously,[48,49] and have been used in all-oxide ZnO/$Cu_2O$ solar cells.[50]

In this work, we have used AP-SALD to integrate $Cu_2O$ layers as HTL in 3x3 cm² SHJ solar cells (see supporting information and Fig.SI1 for details on the deposition system and parameters used and for details on the fabrication of the SHJ cells). The effect of the HTL deposition temperature and thickness on the passivation, recombination level, and output results after each step of the solar cell fabrication has been evaluated. Moreover, the obtained results are rationalised by performing a fitting two-diode model on the IV curves. Our cells present record efficiencies when compared to other Si-based solar cells incorporating $Cu_2O$ layers. Especially appealing is the large area for which our results have been obtained.

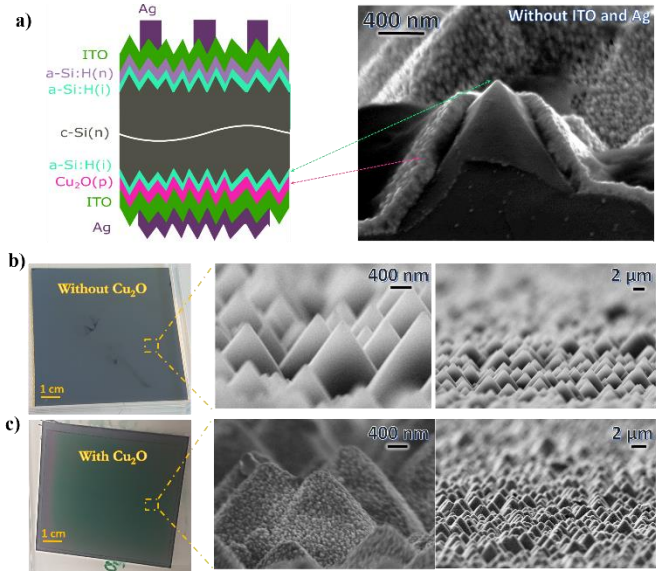



**Fig.1** (a) Schematic diagram of $Cu_2O$ HTL based solar cells and a cross-section SEM of $Cu_2O$ film on top of textured silicon surface without ITO and Ag contacts. (b) Optical (left) and SEM (middle and right) images of bare a-Si:H(i) without $Cu_2O$ thin film deposited on top of textured SHJ with a cross section zoom over the rear bare Si side. (c) Optical and SEM images of the SHJ architecture with a zoom over rear side of the coated 200 nm $Cu_2O$ HTL on Si pyramids and the front side of SHJ.

Fig. 1a shows the structure of SHJ cells incorporating $Cu_2O$ HTL layers. Similarly to the reference SHJ devices, the front side ITO transparent electrode enables carrier collection and improved conduction to the metallic electrodes.[51] Besides, it also acts as an anti-reflective layer.[22] A cross-section SEM picture also illustrating the bottom part of the cell is also included, where the $Cu_2O$ is clearly observed. Fig. 1b and Fig. 1c show optical images of the bare device rear side (with no ITO/Ag contacts), without and with a 200 nm thick $Cu_2O$ layer on top of the textured silicon surface. The figure also shows the corresponding tilted cross-section SEM views. The $Cu_2O$ layer is conformal over the textured Si surface (pyramids) and appears continuous and free of pinholes, which is a prerequisite to minimize shunt-related defects.

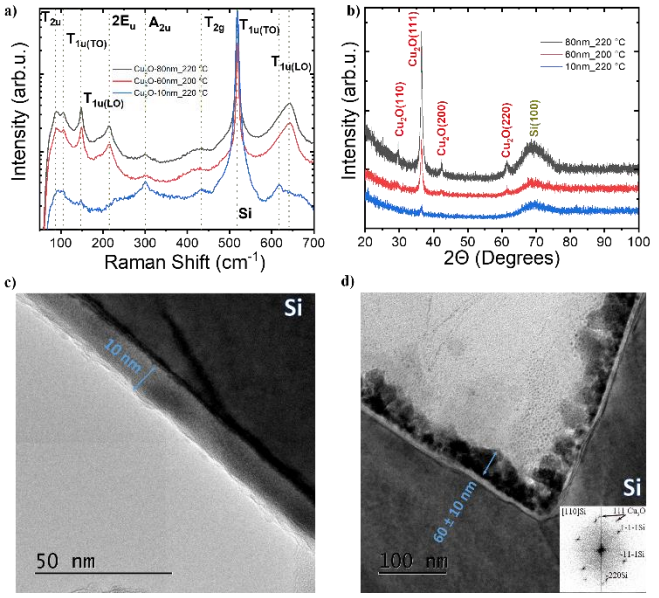



**Fig.2** (a) Raman Spectra of $Cu_2O$ thin films deposited at different temperatures on the SHJ cell, obtained with a 488 nm laser. The typically observed Raman modes for $Cu_2O$ are included as reference. (b) XRD pattern of ~~the~~ 80 nm, 60 nm, and 10 nm thick $Cu_2O$ film deposited on top of the SHJCs at 220 °C and 200 °C, and cross-section TEM images of (c) the 10 nm (d) and 60 ± 10 nm thick $Cu_2O$ films. The inset in (d) shows a selected-area electron diffraction (SAED) pattern.

In our study, 10 nm, 60 nm, and 80 nm thick $Cu_2O$ films were deposited either at 200 °C or 220 °C. Raman spectroscopy indicates no presence of other phases (CuO and/or Cu), as shown in Fig. 2a. The intensity of the peaks observed is mostly the result of film thickness. Further study on that aspect was performed using X-ray diffraction (XRD) measurements for samples with a thickness of 80, 60, and 10 nm, as shown in Fig. 2b. The samples were titled during the measurement by 3 degrees to diminish the effect of the silicon signal and the cuprous oxide on top is observed to be crystalline in all cases, in agreement with Raman data, with a preferential texture orientation along the (111) plane, which corresponds to the reflection at 36.28° (referenced to the ICSD26963 database).[52] The difference in peak intensity between the 80 nm and 60 nm films is mainly due to the different deposition temperature and resulting crystallinity.[48] In the case of the 10 nm films, the low intensity is mainly due to the low thickness of the film. (XPS was also performed to rule out the presence of traces of CuO or Cu in the film. The results confirm that the films only contain $Cu_2O$, as shown in Supplementary Fig.SI2). Fig. 2c & 2d shows the cross-section TEM analysis of the $Cu_2O$ deposited on top of the SHJ cells, for 10 nm and 60 nm thick $Cu_2O$ HTL. The images confirm that the films do not present cracks nor pinholes and that they follow the profile of the textured Si in a very conformal fashion.

One of the main concerns while integrating $Cu_2O$ HTL into SHJ cells is the passivation quality, which should be conserved after the deposition process to allow reaching a high open-circuit voltage (*Voc*). Fig. 3a and 3b show photoluminescence (PL) images of both standard cells with an a-Si:H(p) layer and cells with a 10 nm $Cu_2O$ HTL. PL data was obtained at different stages: before $Cu_2O$ deposition and after the deposition of ITO and the silver contact. PL intensity can be directly converted to the absolute excess Minority Carrier Densities (MCDs).[53] The *Voc* value is in turn related to the excess MCDs $\Delta n$ and $\Delta p$ (considering: $\Delta p = \Delta n$) by the equation:[54] $implied\ Voc = (\frac{kT}{q})ln(\frac{(N_d+\Delta n)\Delta n}{n_i^2})$ where $N_d$ is the doping concentration, $n_i$ is the intrinsic carrier concentration, *k* the Boltzmann constant (≈8.617x10$^{-5}$ eV/K) and *T* is temperature (K). Therefore, an implied *Voc* can be quantitatively estimated from PL data. With the presence of $Cu_2O$ HTL, it appears that the PL intensity was lower at some local areas, indicating a lower excess MCD in these regions as a result of a higher recombination. In addition to PL measurements, carrier recombination has also been evaluated with a WTC120 instrument from Sinton. After the deposition of the $Cu_2O$ HTL, minority carrier lifetimes and the corresponding implied *Voc* at specific $MCD = 10^{15} cm^{-3}$ were reduced from 2140 µs and 736 mV to 1156 µs and 729 mV, respectively, as shown in Fig. 3d. The values obtained for the reference cell with a-Si:H(p) and without ITO/Ag contact is equal, however, to 1858 µs and 733 mV respectively. Thus, it can be concluded that the SALD deposition did not degrade drastically the passivation properties during the growth of the 10 nm thick $Cu_2O$ film, since the *implied-Voc* stays almost the same with a reduction of the lifetime values. This is in agreement with previous reports on the deposition of ZnO layers by AP-SALD on SHJ cells.[44] For thicker $Cu_2O$ layers, we found strong PL intensity reduction on the sample borders, in the regions covered by the hard mask (See Fig.SI3). In addition, transportation and more handling of the samples was required for the SALD coating, which could have caused further damages on the cells incorporating the $Cu_2O$ HTL as compared with the standard cells.

It can be seen from Fig. 3c that there is almost no lifetime value change after ITO deposition for the reference sample at MCD >10$^{15}$ cm$^{-3}$, while it is reduced as MCD <10$^{15}$ cm$^{-3}$, as often observed in the literature.[55] Similarly, on Fig. 3d, we can observe that almost no further change in the lifetime measurements is observed after ITO deposition on top of the $Cu_2O$ HTL over the full MCD range. This could be related to the slight protection provided by the 10 nm (or thicker) $Cu_2O$ layer from ITO sputtering process damages.[56] Even though the passivation quality of the $Cu_2O$ based SHJ cell is lower than the reference one, samples with $\tau_{eff} \approx 1156\ \mu s$ and implied $iV_{oc} \approx 729\ mV$ still remain acceptable for SHJ cell finalization. Indeed, these values fall in the same order of magnitude of the a-Si:H(p) SHJ (only 4 mV lower), showing that replacing this latter layer by a $Cu_2O$ HTL does not affect significantly the passivation properties at the c-Si/a-Si:H(i) rear interface.

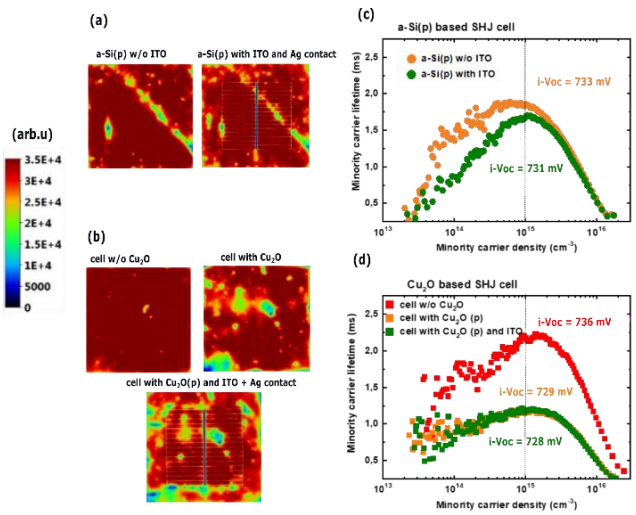


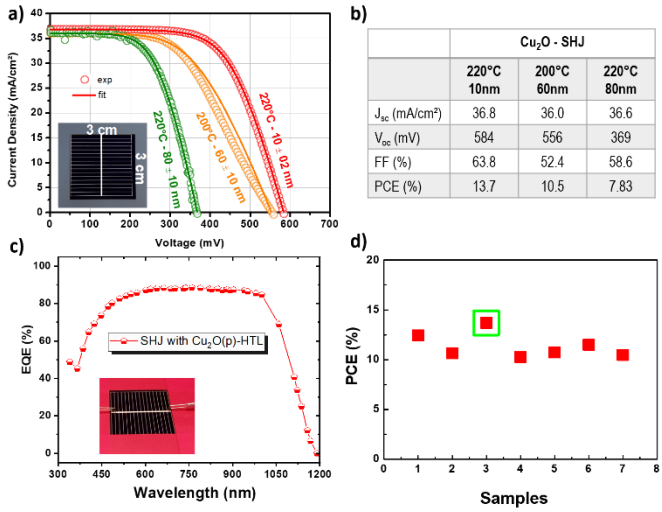

**Fig.3** PL maps of (a) a-Si:H(p) HTL based SHJ cell: before/after the deposition of ITO and the Ag contacts, and (b) 10 nm $Cu_2O$ HTL based SHJ cell: before/after $Cu_2O$ and before/after the deposition of ITO and the Ag contacts; The scale bar represents the PL intensity in arbitrary units. The corresponding carrier lifetime measurements are followed at each stage of (c) a-Si:H(p) based and (d) $Cu_2O$ based SHJ cell. Minority carrier lifetime (MCL) of each measurement on 9 cm² aperture area was taken at typical minority carrier density MCD = 10$^{15}$ cm$^{-3}$ (indicated by a dotted black line). The corresponding i-Vocs were also indicated.

All the $Cu_2O$ HTL with different thickness were thus integrated into complete SHJ cells and the performances were evaluated. The *IV* curves and a table summarizing the obtained cell parameters are presented in Fig 4a and 4b. In the best case, i.e. for the SHJ cell with a 10 nm thick $Cu_2O$ HTL, a *Voc* of 584 mV and a *Jsc* of 36.8 mA/cm² could be obtained, leading to a maximum power conversion efficiency (*PCE*) obtained on the 9 cm² inverted emitter prototype is 13.7%. EQE (External Quantum Efficiency) measurements were conducted on the best sample, as shown in Fig. 4c. The obtained EQE is very similar to the one obtained for the standard cell incorporating an a-Si:H(i) layer (Fig SI3), especially in the infrared range where the replacement of a-Si:H(i) by $Cu_2O$ was expected to have more impact. The *Jsc* values calculated from the EQE data are 35.8 mA/cm² and 36.4 mA/cm² for the $Cu_2O$ and the a-Si:H(p) based cells, respectively. These values are in good agreement with the values obtained from the *JV* measurement. The small difference could be related to a slight variance of hard mask manual positioning when doing the different characterizations (note that the silver contacts accounts for 5.8% of the aperture area).

A small difference in *Jsc* (~0.5 mA) is observed between the two samples (FigSI3) where EQE is slightly smaller at the green-blue range but may be related to poor signal to noise ratio for the very first acquisition point (340 nm). In addition, good surface passivation and moderately high carrier lifetime contributed to the *Jsc* in this rear emitter configuration. However, the *Jsc* can be still improved by reducing recombination and optimizing the front metal grid design to reduce shading with a potential gain of 0.8% shading reduction.

A limiting parameter for the efficiency is the Fill Factor (*FF*). The reported *FF* for our best device is 63.8%, which is comparable to 66.2% and 66.3%, reported for perovskite solar cells incorporating a $Cu_2O$ HTL,[35,38] and is much higher than the maximum reported value of 40.6% for $Cu_2O$ HTL integrated into Si-based devices.[39] However, this value is sensibly lower than the typical 78%-84% generally reported for crystalline silicon based devices. Furthermore, the obtained fill factor value is

mainly correlated to the large contribution of the series resistance between (i) a-Si:H(i)/$Cu_2O$ and/or $Cu_2O$/ITO interfaces that could be decreased by optimizing further the growth conditions.




| | $Cu_2O$ - SHJ | | |
|---|---|---|---|
| | 220°C 10nm | 200°C 60nm | 220°C 80nm |
| $J_{sc}$ (mA/cm²) | 36.8 | 36.0 | 36.6 |
| $V_{oc}$ (mV) | 584 | 556 | 369 |
| FF (%) | 63.8 | 52.4 | 58.6 |
| PCE (%) | 13.7 | 10.5 | 7.83 |

**Fig.4** (a) J-V characteristics (measured under 1 sun) of SHJ cells integrating different $Cu_2O$ HTL and the corresponding fitting curves. Inset: picture of the 9 cm² active cell. (b) Cell performances of the devices in (a). (c) EQE measurement (average over 3 successive measurements) of the SHJ cell incorporating a $Cu_2O$ HTL deposited at 220 °C with a 10 nm thickness. The inset depicts a picture of the cell during measurement. (d) PCE obtained for different samples. Values above 10% were obtained for all seven cells measured, with a best efficiency of 13.7% being obtained [green square]. Note that the front metal grid shadowing is estimated to 5.8% and could be further optimized for Jsc enhancement.

The influence of the $Cu_2O$ on deposition temperature on the performance of integrated SHJ devices was investigated. *JV* curves of samples with $Cu_2O$ deposited at different parameters are presented in Fig.4a, and show that for lower deposition temperatures and thicker HTL layers, the performance of the cell is decreased. In order to rationalise these results, a two-diode model was used to fit the relation between the current J and voltage V[57,58] (see the used equivalent circuit in Fig.SI5):

$$J(V) = J_{ph} - J_{01}\left\{exp\left[\frac{q(V+J*R_s)}{n1*kT}\right]-1\right\} - J_{02}\left\{exp\left[\frac{q(V+J*R_s)}{n2*kT}\right]-1\right\} - \frac{V+J*R_s}{R_{sh}}$$

where $J_{ph}$, $J_{01}$ and $J_{02}$ are photogeneration, diode saturation current densities, respectively. $R_s$ and $R_{sh}$ are denoted for series resistance and shunt resistance; $n_1$ and $n_2$ are diode ideality factors; $k$ and $T$ are Boltzmann constant and temperature, respectively.

The fitting data, displayed in Table 1, show that the diode saturation current densities as well as the ideality factors are in the same order of magnitude as reported for the two-diode model.[58] This accounts for the high short-circuit current for all studied SHJ cells either with a-Si:H(p) or $Cu_2O$ HTL. It should be noted that the diode saturation current densities and shunt resistance vary very little from one sample to another.

Interestingly, the cell with a 60 ± 10 nm thick $Cu_2O$ HTL deposited at 200 °C shows the highest series resistance. This is in agreement with an increase in resistivity of $Cu_2O$ thin films when decreasing the deposition temperature with AP-SALD[48,49]. Therefore, we consider that series resistance is one of the main parameters limiting the cell performance. On the other hand, in some occasions the *JV* curve presents a small S-shape which possibly stems from the counter-diode effect where the interface ITO(n)/$Cu_2O$(p) electrically acts as a parasitic p-n junction. In addition, it can be seen from the *JV* curve (Fig.4a, green curve) that the last sample deposited at 220 °C together with a higher number of deposition cycles (80 nm) can degrade further the cell. The decrease of *Voc* (down to 369 mV) might result from a suppression in passivation due to longer AP-SALD deposition time. In the same line, It has indeed been shown that the short deposition times offered by AP-SALD have allowed to deposit buffer layer oxides, at temperatures up to 180 °C, on sensitive hybrid perovskite cells without degrading them.[37,59]

**Table 1** Fitted parameters of *JV* curves using two-diode model for SHJ cells with different $Cu_2O$ HTL deposition conditions (the associated curves are depicted in Figure 4a).

| | J-V Fitting Results | | |
|---|---|---|---|
| **$Cu_2O$ Temperature-Thickness** | **220°C-10nm** | **200°C-60nm** | **220°C-80nm** |
| **Temperature (T), K** | 300 | 300 | 300 |
| **Diode Ideality Factor ($n_1$)** | 1 | 1 | 1 |
| **Diode Ideality Factor ($n_2$)** | 2.05 | 1.7 | 1.12 |
| **Current Density ($J_{01}$), A/cm²** | $3.20\times10^{-12}$ | $3.00\times10^{-12}$ | $2.00\times10^{-12}$ |
| **Current Density ($J_{02}$), A/cm²** | $1.90\times10^{-07}$ | $9.00\times10^{-06}$ | $1.00\times10^{-07}$ |
| **Shunt resistance (Rsh), Ω.cm²** | $7.00\times10^{04}$ | $8.00\times10^{04}$ | $5.00\times10^{04}$ |
| **Serial Resistance (Rs), Ω.cm²** | 2.65 | 4 | 1.85 |

Our results represent the best efficiency value ever reported for a Si-based solar cell using $Cu_2O$ as a hole transporting or buffer layer. Indeed, several works have been reported on doped and undoped $Cu_2O$ being integrated in cells based on c-Si. Markose et al. have reported a sputtered boron-doped and undoped $Cu_2O$ as a hole-selective layer for c-Si solar cell.[39] The maximum achieved power conversion efficiency was around 5.48% with a reported *Voc* of 114 mV for non-doped films and 370 mV for the doped ones.[39] $Cu_2O$ thin films deposited by sputtering techniques have been widely reported in the literature as hole selective layer in c-Si solar cell structures with maximum efficiency values of 3.39%,[60] and 1.12%.[61] Other approaches have been used to grow $Cu_2O$ and integrate them in Si-based solar cells with a low reported value 0.45% for electro-deposition approaches.[62] The highest reported efficiencies so far are 9.54% using spin-coating approach[40] and 6.02% with the thermal oxidation process.[63] In all cases, the surface areas in these studies varied from 0.01 to 1 cm², thus between 9 and 900 times smaller than for the study presented here. The validation of high efficiency values for large laboratory cells is a key factor towards the large-scale integration of a technology into industrial processes.

Table 2 summarizes the cell parameters, including cell area, for all reported Si-based cells incorporating a $Cu_2O$ layer, along with our results while Fig.5 focuses on the differences in terms of efficiency, $J_{sc}$ and area for the different reports. To sum up, most of the other deposition techniques require a high thermal budget in the case of the thermally oxidized films or complex processes such as sputtering (more damages, vacuum required) and spin coating as well as electrochemical techniques that provide hardly uniform films over the surface substrate (therefore not suitable for up-scaling). Furthermore, the comparison show that the surface area of the $Cu_2O$ deposited by other techniques is always deposited at the laboratory scale

with a smaller surface area (< 1 cm²) which prevents the facile integration to the industrial level. In this work, the HTL layer was deposited over a large surface area of 9 cm² and the resulting solar cell exhibit higher efficiency and current density compared to other Si-based structures. This demonstrates the potential of using the SALD technique to integrate $Cu_2O$ HTL p-type semiconductor for the solar cell devices in the industrial and roll-to-roll processes.

**Table 2** Comparison of our $Cu_2O$ based SHJ with reported Si-based cells incorporating a $Cu_2O$ layer

| Cell type | Deposition methods | Voc (mV) | Jsc (mA/cm²) | FF (%) | PCE (%) | Area (cm²) | Ref. |
|---|---|---|---|---|---|---|---|
| **$Cu_2O$/SHJ** | **SALD** | **584** | **36.8** | **63.8** | **13.7** | **9.0** | **This work** |
| **$Cu_2O$/Si** | sputtering | 114 | 19.39 | 29.2 | 0.64 | 1.0 | 39 |
| **$Cu_2O$:B/Si** | sputtering | 290 | 33.60 | 40.1 | 3.9 | 1.0 | |
| **$Cu_2O$:B/SiOx/Si** | sputtering | 370 | 36.50 | 40.6 | 5.48 | 1.0 | |
| **$Cu_2O$/Si** | Spincoating | 528 | 30.08 | 60.01 | 9.54 | - | 40 |
| **$Cu_2O$:Na/Si** | ED | 480 | 2.20 | 47.0 | 0.45 | - | 64 |
| **$Cu_2O$/Si** | TE | 490 | 28.60 | 42.85 | 6.02 | 0.1 | 63 |
| **$Cu_2O$/Si** | sputtering | 328 | 11.90 | 50.5 | 1.97 | 0.019 | 60 |
| **$Cu_2O$/$SiO_2$/Si** | sputtering | 528 | 13.20 | 48.6 | 3.39 | 0.019 | 60 |
| **$Cu_2O$/Si** | sputtering | 420 | 7.80 | 44.0 | 1.12 | 1 | 61 |

ED: Electrodeposited, TE: Thermal Evaporation

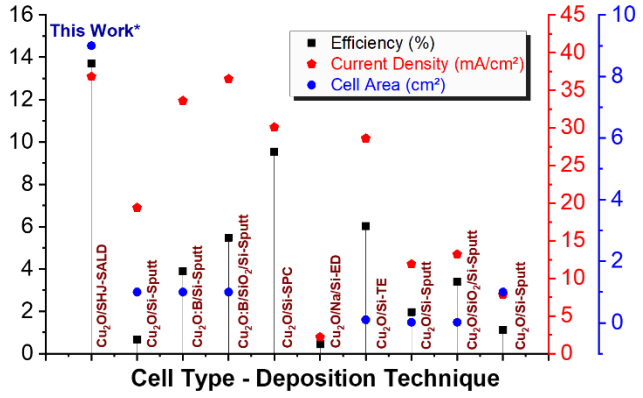



**Fig5** Comparative study of the area, efficiency, and current density of the SALD $Cu_2O$/SHJ structure compared to SHJ in the literature. The compared deposition techniques are: Sputt: Sputtering[39,60,61], SPC: spin coating[40], ED: electro-deposition[64], TE: thermally oxidized[63], SALD: spatial atomic layer deposition.

## Conclusions

In summary, we present the first rear emitter SHJ cell using $Cu_2O$ as a HTL, as a possible alternative to a-Si:H(p). AP-SALD was used to deposit the $Cu_2O$ HTL. Our results show that AP-SALD allows obtaining a conformal and uniform large area of $Cu_2O$ deposited at a low thermal budget without degrading the passivation effect of the a:Si:H(i) layer. The best efficiency obtained was 13.7% on a large-area 9 cm² active cell, with a *Jsc* = 36.8 mA.cm$^{-2}$ and a *Voc* = 598 mV. These values were obtained for a 10 nm thick $Cu_2O$ HTL deposited at 220 °C and are the highest reported to our knowledge for PV devices integrating $Cu_2O$ as HTL in silicon absorber-based devices. These results could be related to the intrinsic high quality of SALD thin films, together with the low deposition temperature that prevents the degradation of the passivation properties at the c-Si/a-Si:H(i) rear interface. Further optimization in the deposition conditions and the corresponding transport properties of the $Cu_2O$ HTL are expected to increase further the efficiency of the device closer to that of standard SHJ. Finally, our work represents a proof-of-concept study of integrating $Cu_2O$ deposited by SALD as HTL in c-Si based PV devices.

## Conflicts of interest

There are no conflicts to declare

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