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Channel width dependent subthreshold operation of tri-gate junctionless transistors

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ABSTRACT

Junctionless transistors (JLTs) are one of attractive candidates for further scaling down thanks to their promising advantages based on a structural simplicity without PN junctions, and their physical operation is quite different from traditional inversion-mode (IM) transistors. In this paper, we investigated the subthreshold operation of tri-gate JLTs with various effective width (W_{eff}) and compared to that of IM transistors. The on current to off current ratio (I_{on}/I_{off}) and subthreshold swing (SS) of JLTs were varied dramatically as changing W_{eff}. In addition, a better immunity against short channel effects (SCEs) of JLTs was proven. Physical operation mechanism on the subthreshold regime was also discussed in detail with considering distribution of mobile charge carriers, maximum depletion width, full-depletion mode, bulk neutral and surface accumulation conduction.

Keywords: tri-gate junctionless transistors (JLTs), subthreshold conduction, width variation, on current to off current ratio (I_{on}/I_{off}), subthreshold swing (SS), maximum depletion width

Multiple gate junctionless transistors (JLTs) are an attractive candidate for the advanced 5 nm complementary metal-oxide-semiconductor (CMOS) technology nodes and beyond, since JLTs have promising benefits based on their structural simplicity without PN junctions at source/drain (S/D) regime [1-4]. Less mobility degradation, improved low-frequency noise behavior and better reliability against bias stress are key advantages of JLTs, thanks to bulk conduction principle and a reduced transverse electric-field (E-field) at operating conditions [5-8]. In addition, the fundamental and technical challenges in the CMOS industry could be overcome by new channel materials such as two-dimensional (2D) transition-metal dichalcogenides (TMDs, MoS_2 and WSe_2), exhibiting unique electrical and optical properties [9,10]. Interestingly, semiconducting multi-layer TMDs transistors have uniformly doped S/D and channel with ohmic-like contacts and bulk neutral conduction, which are very similar to those of planar JLTs [11-13]. The physics of carrier transports in JLTs is quite different from conventional inversion-mode (IM) transistors [5-8,14,15] and in particular, understanding subthreshold conduction mechanism of JLTs is very important for the realization of low power and energy-efficient devices with them [16].

In this paper, the subthreshold operation of tri-gate JLTs with various widths were investigated and also compared to that of traditional IM transistors. Some of free charge carriers could be still remained in JLTs with a wide width even on the subthreshold regime, and they affected significantly overall behavior of on current to off current ratio (I_{on}/I_{off}) and sub-threshold swing (SS). The remained carriers were dramatically vanished in nanowire-like JLTs. Moreover, JLTs have shown a better immunity against short-channel effect (SCEs) in terms of SS values, than IM transistors.

N-type tri-gate JLTs in arrays of 50 channels were fabricated at CEA-Leti on silicon on insulator (SOI) wafer with ≈ 10 nm thick Si (t_{si} ≈ 10 nm). Targeted channel doping concentration with phosphorus was

$N_d = 10^{19}/cm^3$ and IM transistors as a comparison were also fabricated by the exactly same process only except for channel doping process. A detail fabrication process has been reported in previous works [14]. Schematic architecture describes device structures of the fabricated tri-gate JLTs as shown in Fig. 1(a). Channel width differences (ΔW) between on-mask width (W_m) and effective width (W_{eff}) were determined by the transfer length method (TLM) using the linear relationship between drain current and W_m [14] and the extracted values were $\Delta W \approx 55$ nm for JLTs and $\Delta W \approx 60$ nm for IM transistors, respectively. Electrical measurements were done by using 4155A semiconductor parameter analyzer and FlexPDE software was used for numerical simulation results from solving two-dimensional Poisson equations.

Drain current (I_d) was measured from the JLTs with 50 channels and then, was divided by 50. I_d normalized by W_{eff} versus gate voltage (V_g), i.e. transfer curves of tri-gate JLTs and IM transistors were measured with varying W_{eff} in Fig. 1 (b) and (c), individually. Although JLTs shows a clear switching behavior, the off current level (minimum $I_d \approx 10^{-12}$ A/μm) of planar-like JLTs with wide widths was two orders of magnitude higher than that ($\approx 10^{-14}$ A/μm) of IM transistors. The off current (I_{off}) of JLTs was decreased as decreasing W_{eff} and then, it was reduced dramatically close to $\approx 10^{-13}$ A/μm in the nanowire-like JLTs with $W_{eff} = 45$ nm and 25 nm, probably due to enhanced gate controllability in the narrow structure.

There are two kinds of conduction channels such as bulk neutral and surface accumulation channel in JLTs above the flat-band voltage ($V_g > V_{fb}$), while IM transistors have an inversion channel only [5-8]. As decreasing V_g, the accumulation channel at the top interface between Si and gate oxide in JLTs gradually disappeared and only the bulk channel exists at flat-band condition ($V_g = V_{fb}$). For further decreasing V_g ($V_g < V_{fb}$), the bulk channel is squeezed due to the depletion of mobile electrons near the top interface. A strong negative V_g can achieve a full depletion state (ideally, no conduction), if heavily

doped Si channel of JLTs is thinner than maximum depletion width (D_{max}). The D_{max} of a planar-like JLT with considering $N_d = 10^{19}/cm^3$ can be theoretically estimated as ≈ 12 nm by below well-known equation [17]:

$$D_{\max} = 2 \times \sqrt{\frac{\varepsilon_{si} \times kT \times \ln\left(\frac{N_d}{n_i}\right)}{q^2 N_d}} \quad (1)$$

where ε_{si}, q, k, T and n_i means the dielectric constant of Si, the electronic charge, the Boltzmann's constant, the absolute temperature and the intrinsic carrier density, respectively. Although the estimated D_{max} of JLTs is greater than t_{si} = 10 nm, some mobile electrons could be still in existence at bottom interface between heavily doped Si channel and buried oxide (BOX) even for very negative V_g. The remained free electrons could give rise to a higher level of I_{off} in the planar-like JLTs.

Distributions of free carrier concentration per unit volume (n) in the cross-sectional channel of tri-gate JLTs were simulated as shown in Fig. 2. When $V_g \approx 0.5$ V, the entire channel layer from the bottom to the top interface is full of electron charge carriers (bulk neutral state) with $\log_{10}(n) = 19$ (thus $n = N_d$) in orange color. That is the flat-band condition. As increasing V_g > flat-band voltage ($V_{fb} \approx 0.5$ V), an accumulation channel is created at the top interface in red color. In addition, as decreasing $V_g < V_{fb}$, the bulk channel is getting depleted from the top interface. Then, for $V_g = -1.0$ V, the $\log_{10}(n)$ on the whole Si channel was very low (blue color) in the nanowire structure (W_{top} = 10 nm) as shown in Fig. 2(b). However, the planar-like JLTs (W_{top} = 350 nm) in Fig. 2(a) contains some considerable charge carriers (green color, $\log_{10}(n) \approx 16$) near the bottom interface even at $V_g = -1.0$ V. Moreover, the subthreshold current in the narrow JLT flows in the center of the nanowire channel, while that in IM transistor flows in the top corners [18]. Therefore, the corner effect can be negligible on the subthreshold operation in JLTs with the nanowire structure.

Figure 3(a) shows the I_{on}/I_{off} (maximum I_d/ minimum I_d in log scale) with various W_{eff}. The overall I_{on}/I_{off} values of JLTs was lower than those of IM transistors. However, the I_{on}/I_{off} ratio of JLTs increased abruptly for decreasing W_{eff}, while a slight increase was observed on that of IM transistors.

The number of free carriers in traditional IM transistors on the subthreshold regime is too small to form a potential gradient and an electric-field along the channel. Therefore, subthreshold current in the IM transistors is not originated from drift-conduction but from diffusion-conduction due to the gradient of the free electron density along the channel in depletion regime [17]. The diffusion current in the subthreshold regime varies exponentially with V_g and can be given as:

$$I_d \propto \exp\left(\frac{qV_g}{mkT}\right) \quad (2)$$

where m denotes the ideality factor ($m \geq 1$).

Derivatives of $\log_{10}(I_d)$ in IM transistors were plotted with varying W_{eff} as shown in Fig. 3(d). The clear plateau regime verified a typical diffusion dominant conduction with the exponential relationship of I_d vs. V_g. On the other hand, JLTs revealed only a narrow peak shape instead of a plateau as shown in Fig. 3(b) [19]. The few remaining free carriers at the bottom interface in Fig. 2(a) could add a drift-current component to the conventional mechanism of subthreshold conduction, which leads the deviated behavior of JLTs as compared to a typical subthreshold current of IM transistors.

W_{eff} dependence of the subthreshold swing (SS), extracted from $SS = 1000 \times dV_g/d[\log_{10}(I_d)]$, was plotted in Fig. 3(c) for JLTs and 3(e) for IM transistors. For wide W_{eff}, the SS values of JLTs were higher than those of IM transistors. JLTs have a larger equivalent electrical oxide thickness due to the depletion layer under gate oxide during the subthreshold conduction. That also results in the weaker gate controllability of JLTs [20]. However, the SS value of JLTs was getting very close to the ideal value (60 mV/dec) as decreasing W_{eff}.

Figure 4 shows the W_{eff} dependent transfer curves and SS values with short channel lengths. The SS

values of JLTs were comparable to those IM transistors for L_m = 100 nm in Fig. 4(c). However, for the shortest length L_m = 50 nm, a better gate controllability was observed in JLTs, while the SS of IM transistors was raised abruptly due to a strong short channel effects (SCEs). Those results proved that JLTs have a better electrostatic immunity against SCEs in the subthreshold regime [15].

Although planar-like junctionless transistors (JLTs) with t_{si} = 10 nm and N_d = $10^{19}/cm^3$ have demonstrated a clear switching behavior, some free electrons could be still remained at the bottom interface between heavily doped Si channel and buried oxide (BOX) even on the subthreshold operation regime. The remained free carriers gave rise to a higher off-current, a deviated shape of $\log_{10}(n)$ derivatives and a degraded SS value of JLTs, as compared to those of IM transistors. However, the I_{on}/I_{off} ratio and SS of tri-gate JLTs was improved dramatically as reducing effective width (W_{eff}) due to enhanced gate controllability in the nanowire-like structure. Furthermore, the tri-gate JLTs regardless of W_{eff} have shown a better electrostatic immunity against short channel effects (SCEs) in terms of the SS values.

ACKNOWLEDGEMENTS

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FIGURE CAPTIONS

Figure 1. (Color Online) (a) Schematic architecture of the fabricated tri-gate JLTs and the I_d vs. V_g transfer curves with varying W_{eff} of (b) tri-gate JLTs and (c) IM transistors as a comparison. The devices were measured in the linear operation regime with V_d = 50 mV.

Figure 2. (Color Online) Simulated distributions of free carrier concentration per unit volume (n) in the tri-gate JLTs with (a) W_{top} = 350 nm (planar-like) and (b) W_{top} = 10 nm (nanowire-like).

Figure 3. (Color Online) (a) The extracted I_{on}/I_{off} ratio, the derivatives of $\log_{10}(I_d)$ for (b) JLTs and (d) IM transistors and the subthreshold swing (SS) with various W_{eff} for (c) JLTs and (e) IM transistors.

Figure 4. (Color Online) W_{eff} dependent transfer curves with a short channel length (L_m = 50 nm) for (a) JLTs and (b) IM transistors. The devices were measured in the linear operation regime with V_d = 50 mV. (c) Extracted SS values with various W_{eff}.

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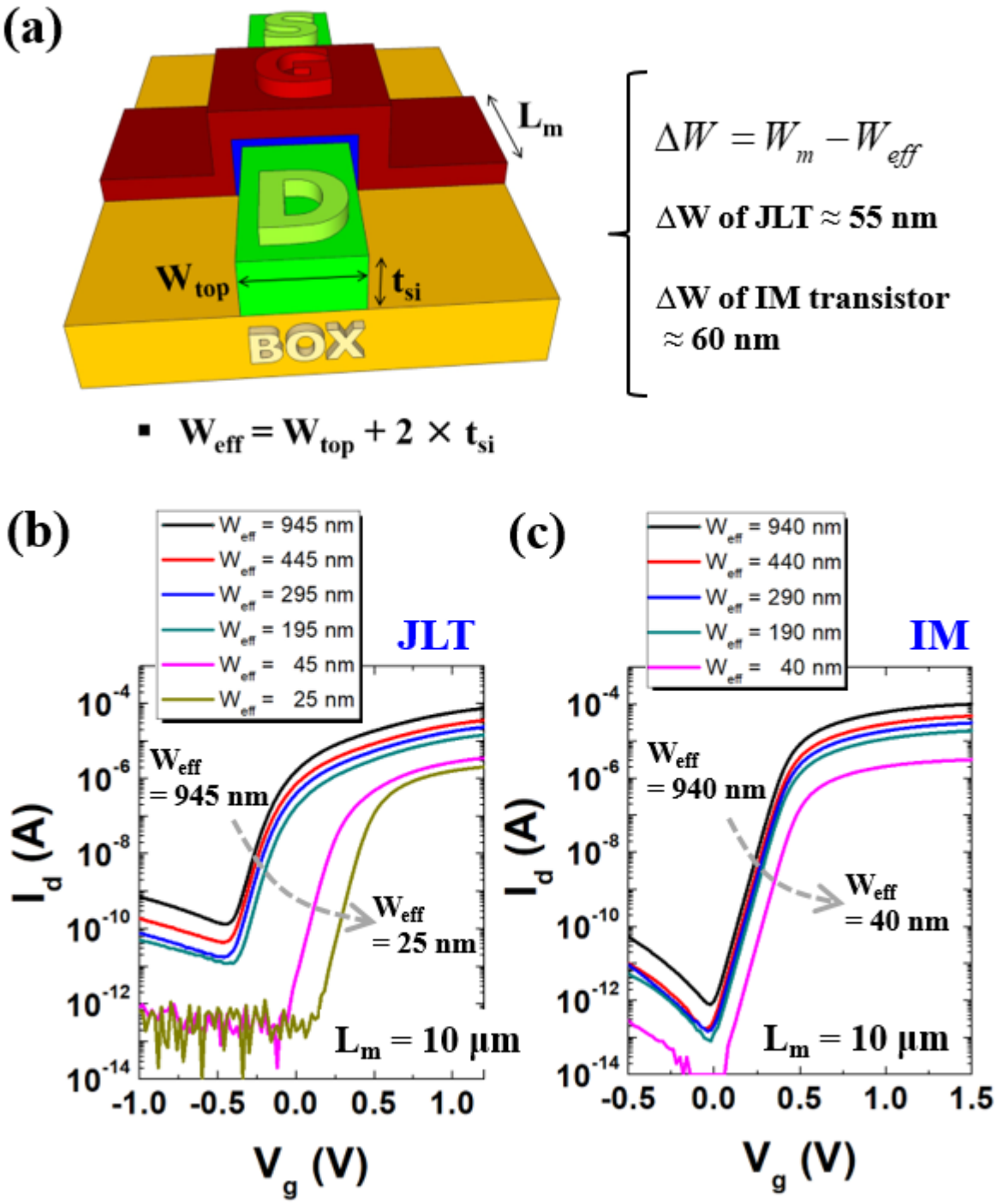

Fig. 1 D. -Y. Jeon et al.

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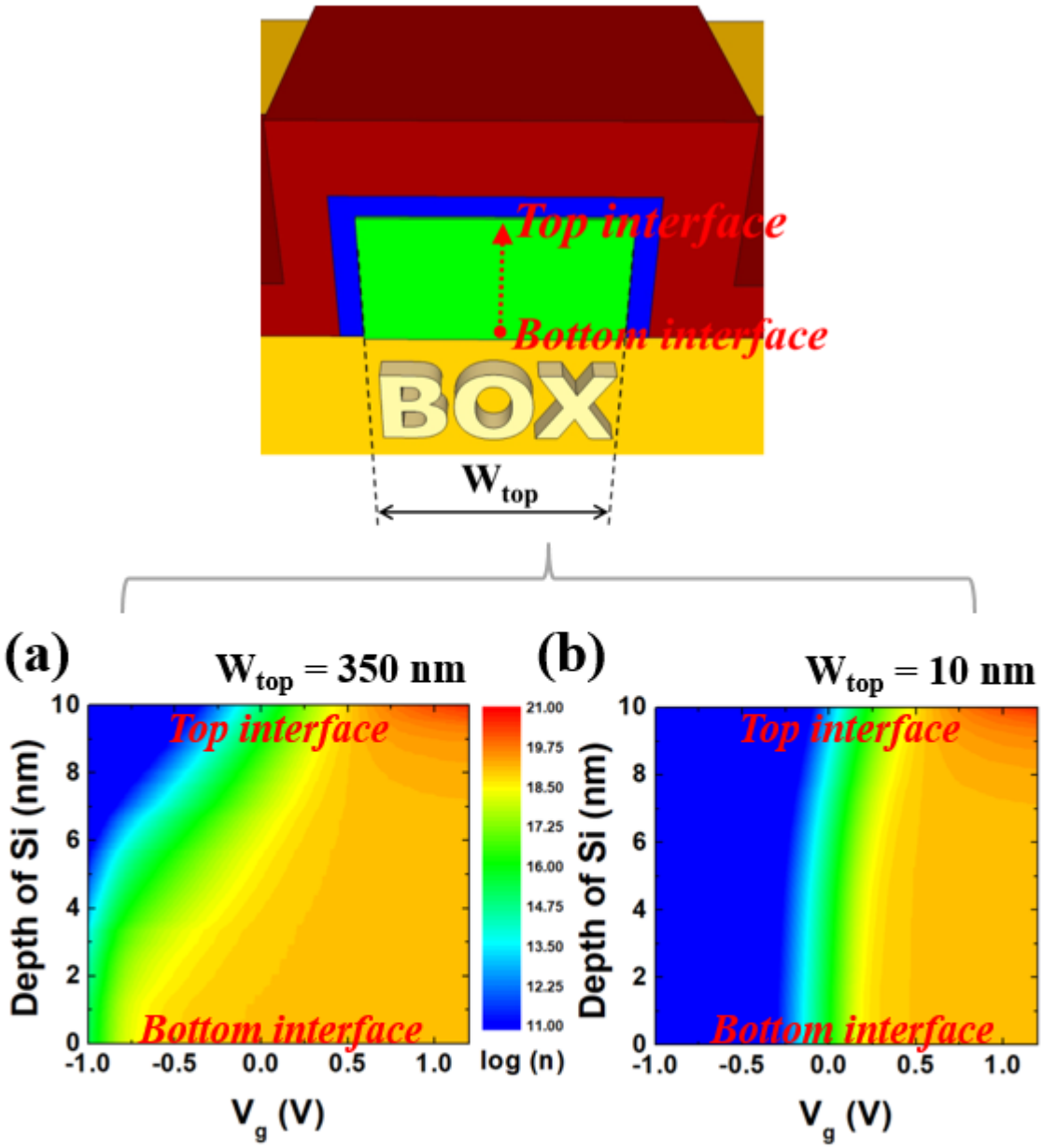

Fig. 2 D. -Y. Jeon et al.

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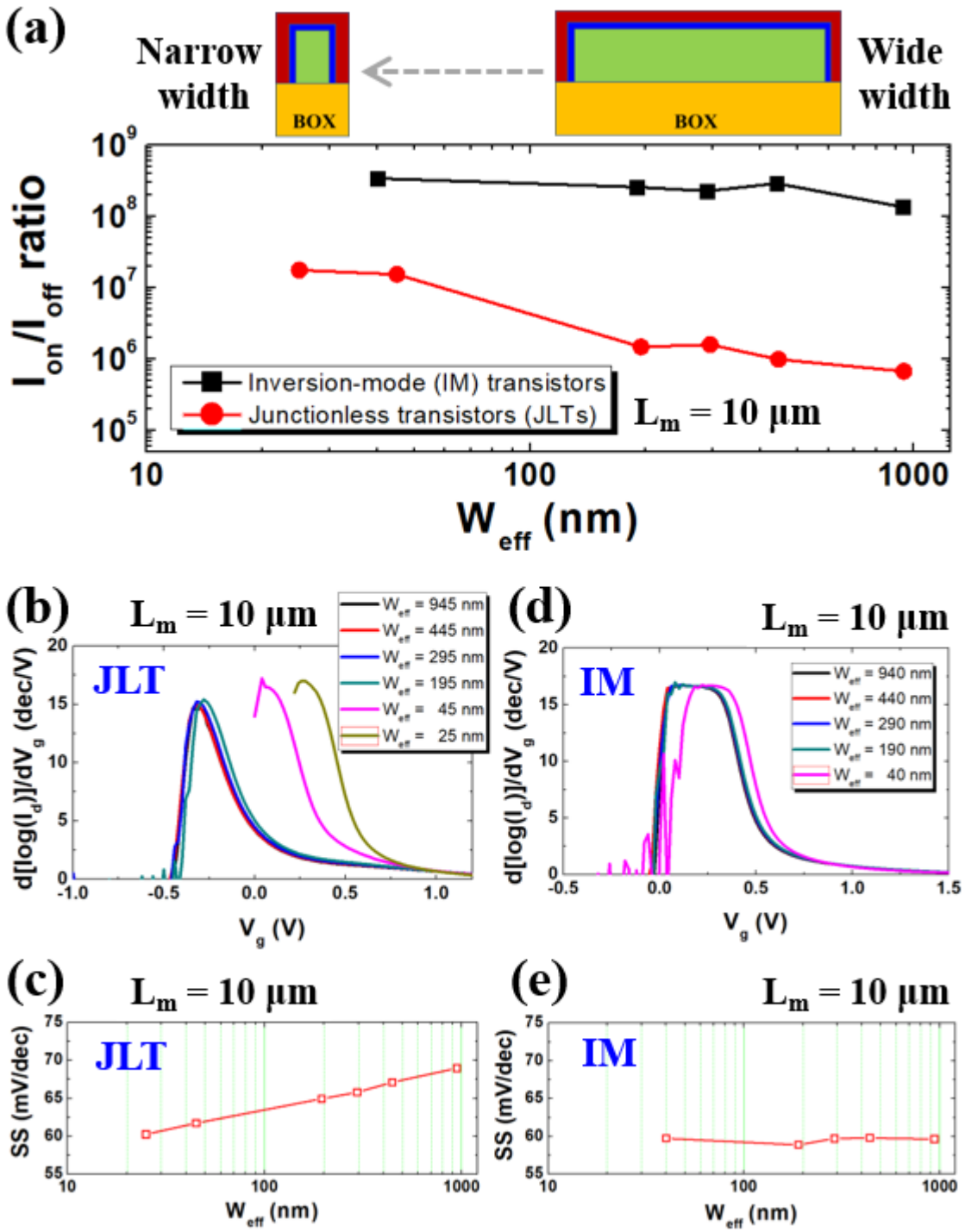

Fig. 3 D. -Y. Jeon et al.

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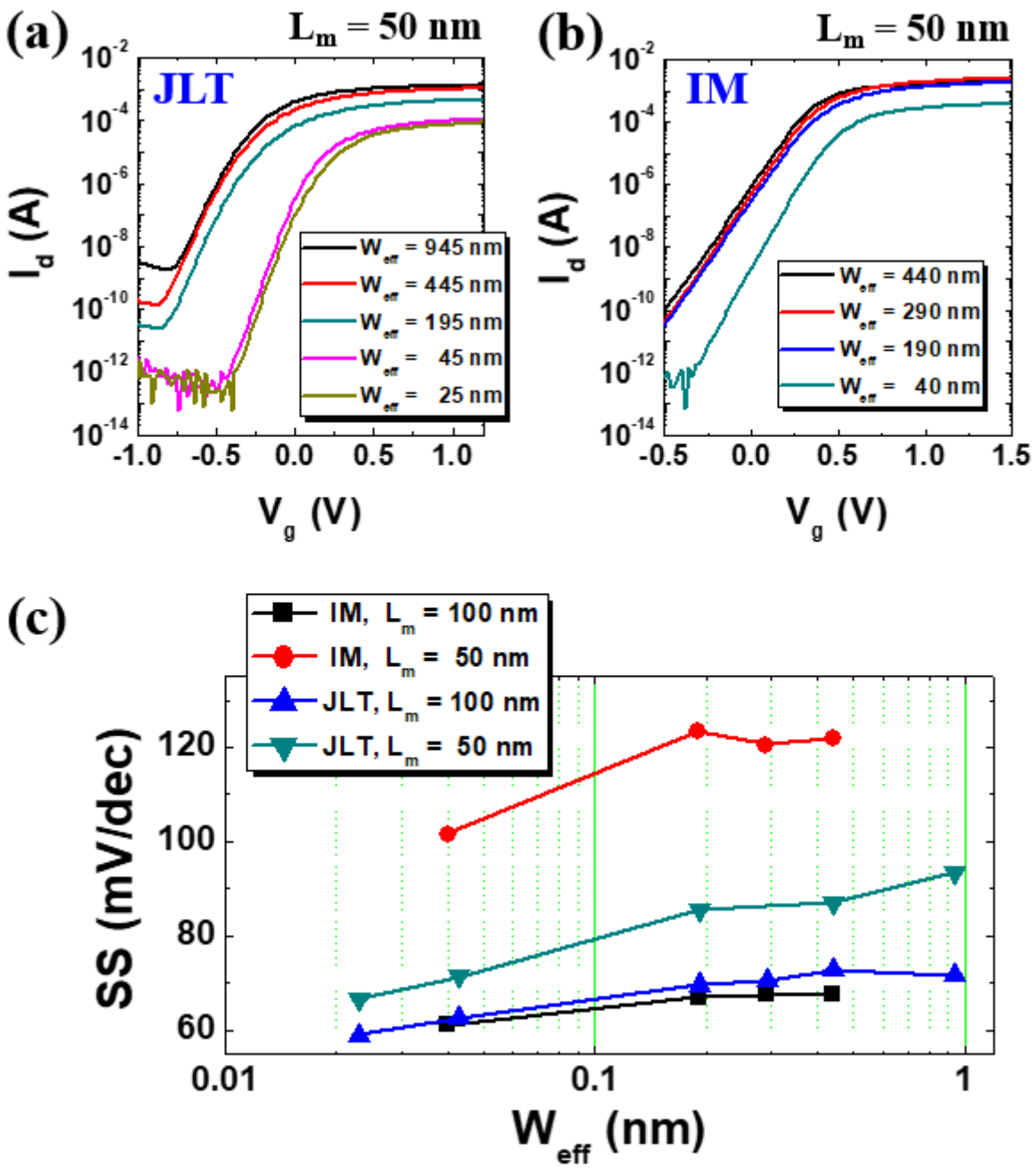

Fig. 4 D. -Y. Jeon et al.