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Abstract— **In this paper, we compare the evolution with temperature of the experimental characteristics of Nanonet-based Field-Effect Transistors, with a modelling of carrier transport in the percolating regime. The main electrical parameters of Nanonet-based Field-Effect Transistors that featured different nanowire densities and source-drain distances were extracted from static measurements at different temperatures. The temperature dependence of low field mobility and threshold voltage was explained by the temperature activated behaviour of inter-nanowire junctions, and the activation energy dispersion of individual junctions. A Monte-Carlo simulation of Nanonet FET in the shape of a random percolating network of resistances and thermally activated junctions was used to confirm the influence of activation energy dispersion on low field mobility. The simplest model which was able to capture experimental trends consisted in a bimodal distribution of activation energies, with a subset of non-thermally activated junctions (resistive junctions) while other junctions were thermally activated (energy barriers at the junctions).**

Random network; silicon nanowire; electronic transport; compact model; percolation; energy barrier; Monte-Carlo simulation; low temperature

1. INTRODUCTION

Nanonet (NN) is a random network of nanowires (NWs). Because Si-NN is made of Si-NWs, an important sensitivity to surface charges is expected, which can be used for sensing applications.[1] In addition, contrary to NW FET [1,2] and GAA FET [3, 4, 5], Si-NN Field Effect Transistor (FET) can be fabricated without requirement of high-resolution lithography techniques or elaborated process technology.[6] Furthermore, Si-NNs can be transferred on any kind of

substrate, which make them perfectly suitable to the 3D integration of sensors, with direct vertical wiring to the CMOS conditioning and readout electrics, or to an integration on flexible substrates.[7] The first NN structures have been made with other materials than silicon, for example carbon nanotubes (CNT)[8, 9] and ZnO nanowires.[10] These structures, especially CNT NN-FETs have been deeply studied with static, RF measurements[11] and low frequency noise measurements.[12] However, some characteristics of the CNT-based nanonets make them quite different from the silicon based nanonets. One important feature of the former comes from the respective roles of metallic and semiconducting CNTs on transport.[13] Moreover, the contacts between CNTs have rather been modelled with Variable Range Hopping.[14] Conduction through a ZnO nanonet has been recently studied for chemiresistive detection applications with a focus on the analysis of the I_d-V_d characteristic under the influence of barrier height modification at nanowire-nanowire junctions.[15]

Until recently, the main technological roadblock to the fabrication of Si-NN FETs has been the presence of non-conductive junctions between Si-NWs, due to the presence of native silicon dioxide layer at their interface.[6] For this reason, Si-NN was known to be insulating for channel lengths larger than NW length.[6] As a result, Si-NN FETs have been mainly used in devices featuring a maximal channel length close to the length of a single NW. For the same reason, there has not been yet deep studies of the transport through a random network of silicon nanowires, nor measurement of the electrical characteristics of the junctions. The detrimental effect of the native oxide at the junctions has been lately solved with a sintering at low temperature, compatible with CMOS integration[16], leading to the first integration of Si NN. in a back gated transistor architecture.[17] This Si-NN FET has been extensively characterized through static measurements. It has been shown that a combination of percolation and dispersion effects was required to understand the dependence of static characteristics with channel length and with the density of nanowires in the nanonet. Especially, it has been explained how nanowires threshold voltage dispersion explains the variation of subthreshold slope and threshold voltage of the NN FET with geometry and NW density.[18] Si-NN FET has been then modelled as a NW network with a random dispersion of threshold voltage.[19] More recently, Si-NN FETs have been characterized through low frequency noise measurements.[20] In this paper, Si-NN FET were characterized through static electrical measurements at different temperatures. Experimentally, we found that ON-current and mobility were varying with temperature in significantly different ways, depending on channel length and nanowire density. These trends cannot be

explained without assuming that there is a potential barrier at the interface of at least some NW/NW junctions. In this paper, the understanding of this behaviour is assessed with the help of Monte-Carlo simulations of Si-NN where inter-nanowire junction resistance is accounted for. Our aim here is not to provide a fit to experimental results but to identify the origin of the observed trends.

2. FABRICATION

The process of Si-NN fabrication and their integration into back gate field effect transistor has been described elsewhere.[21, 22, 23] The NNs used in this study (Fig.1-(a)) were self-assembled from Si-NWs grown by Vapor Liquid Solid chemical vapor deposition. NW length and diameter were respectively 7 µm ± 3 µm and 40 nm ± 7 nm. NNs can be fabricated with different NW densities.[24] For this paper, several NNs were fabricated with 4 different values of nanowire density d_{Wires} (from 0.28 NWs.µm^{-2} to 0.65 NWs.µm^{-2}). They were then transferred on a Si / Si_3N_4 wafer. This material was chosen instead of the more commonly used SiO_2 for technological reason. Indeed, junction sintering is prepared by the removal of the native oxide surrounding the nanowires by an HF-based Buffered Oxide Etching (BOE) step which would remove the back-gate oxide and short-circuit gate and channel. Thermal annealing at 400 °C was performed to improve electronic transport through the network, by means of NW-NW junctions sintering.[16, 21] Then, Si-NNs were passivated with a 8 nm thick Al_2O_3 layer using Atomic Layer Deposition[22] and finally contacted by Ni/Au metal pads using a lift-off technique associated with local removal of Si_3N_4 by HF treatment in contact pad openings. Field-effect control was obtained by using the Si / (200nm) Si_3N_4 substrate as a back gate. Finally, a last thermal annealing at 400 °C was realized to promote silicide formation at the interface between Si NWs and metal contact pads.[21] Several device geometries were available with Source-Drain distance L_{mask} ranging from 5 µm to 1000 µm and a constant pad width W_{mask} = 200 µm (Fig.1-(b)).

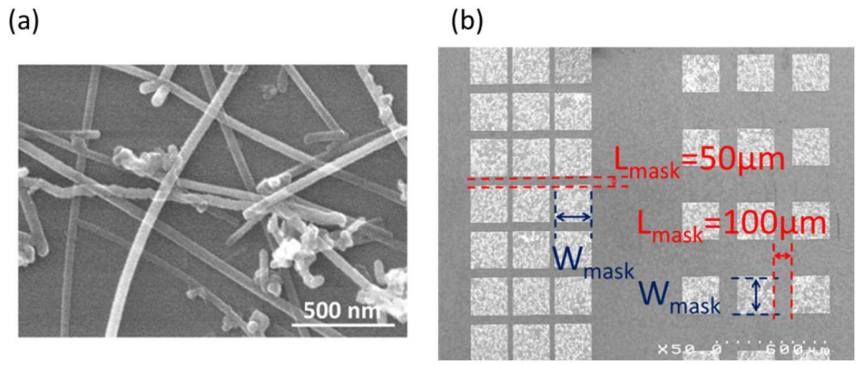
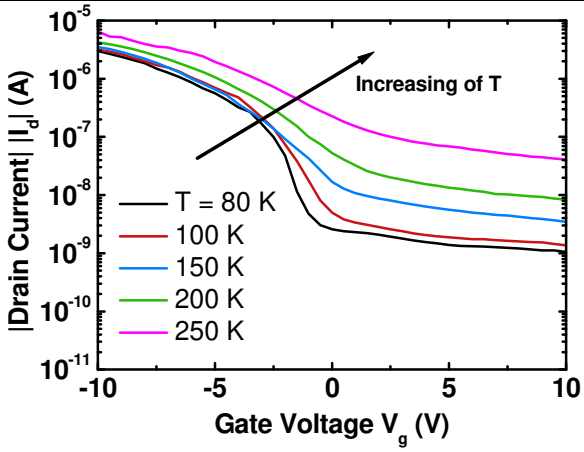
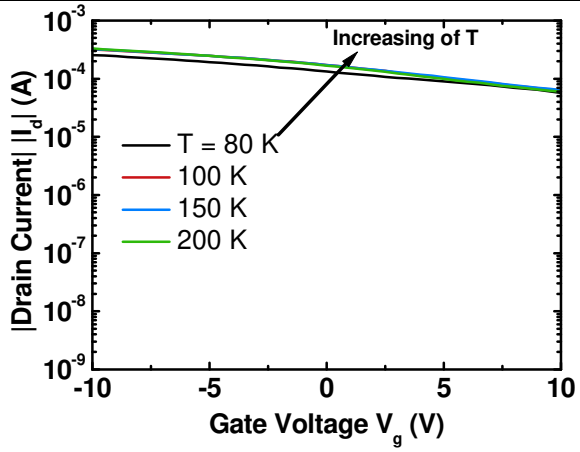
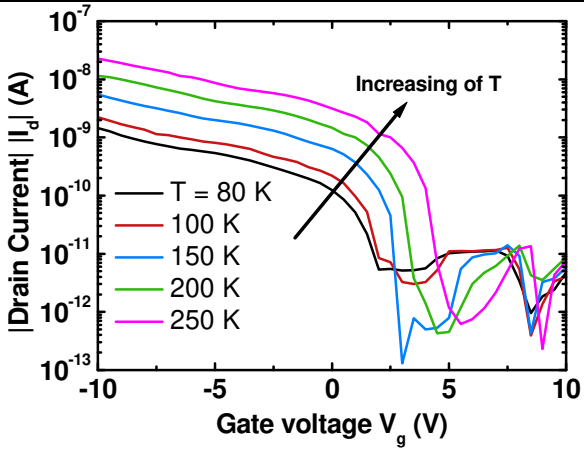
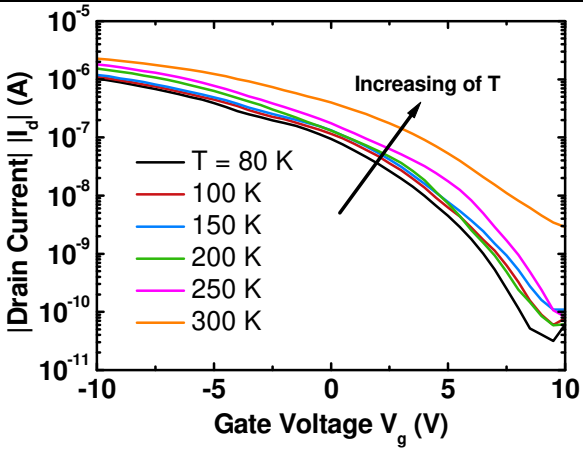


Figure 1. *(a) SEM image of a nanonet made of VLS grown Si-Nanowires after passivation step [22]. (b) Top view SEM image of the fabricated devices [18]*

3. EXPERIMENTAL PROTOCOL AND RESULTS

NN FETs were characterized using a Süsstec cryogenic probe station, where temperature could be varied between 80 K and 400 K. An HP 4155A semiconductor parameter analyzer was used to measure drain current (I_d) as a function of the voltage applied on the backgate (V_g) with the source contact linked to the ground and a constant voltage (V_d = -4 V or V_d = -9 V) applied to drain. Figs.2-(a) and 2-(c) show typical transfer characteristics of two devices (with L_{mask} = 5 µm and L_{mask} = 50 µm, respectively) for different temperatures for the smallest studied density (0.28 NWs.µm^{-2}). Figs.2-(b), 2-(d) and 2-(e) are plotting transfer characteristics of three devices (with L_{mask} = 5 µm, L_{mask} = 50 µm and L_{mask} = 1000 µm respectively) for different temperatures for the largest studied density (0.65 NWs.µm^{-2}). An increase of drain current with density is visible at constant temperature and constant source-drain distance, which can be explained by the increase of the number of paths bridging source and drain. This increase has been explained in [18] for Si-NN FET and is a well-known result for metallic nanonets [25] and CNT NN FETs.[9] This variation is nonlinear and can be modelled with a power law using percolation theory for a 2D stick network.[26] However the detailed analysis of this dependence would require more statistical measurements and is outside the scope of this paper. Short devices (L_{mask} = 5 µm) have a S-D distance smaller than NW length (7 µm) and the channel consisted essentially in NWs linking directly S and D, with negligible role of NW-NW junctions. In contrast, with a S-D distance (L_{mask} = 50 µm or L_{mask} = 1000 µm) much larger than the average NW length (7 µm), the percolating conduction paths between source and drain involved several NWs, connected by sintered NW-NW junctions, in series. Comparison of Fig.2-(a) with Fig.2-(c) reveals that the transfer characteristics dependence with temperature was strongly influenced by source drain

distance. The same trend was found with a larger density (compare Figs.2-(b), 2-(d) and 2-(e)). Moreover, comparison of Fig.2-(a) with Fig.2-(b) shows that the temperature dependence of the transfer characteristics varied with NW density: temperature influence decreased when density increased.

	Nanowire density d_{Wires} = *0.28 NWs.µm^{-2}*	Nanowire density d_{Wires} = *0.65 NWs.µm^{-2}*
L_{mask} = 5 µm (« nanowires in parallel »)	 (a)	 (b)
L_{mask} = 50 µm (« percolating nanonet »)	 (c)	 (d)

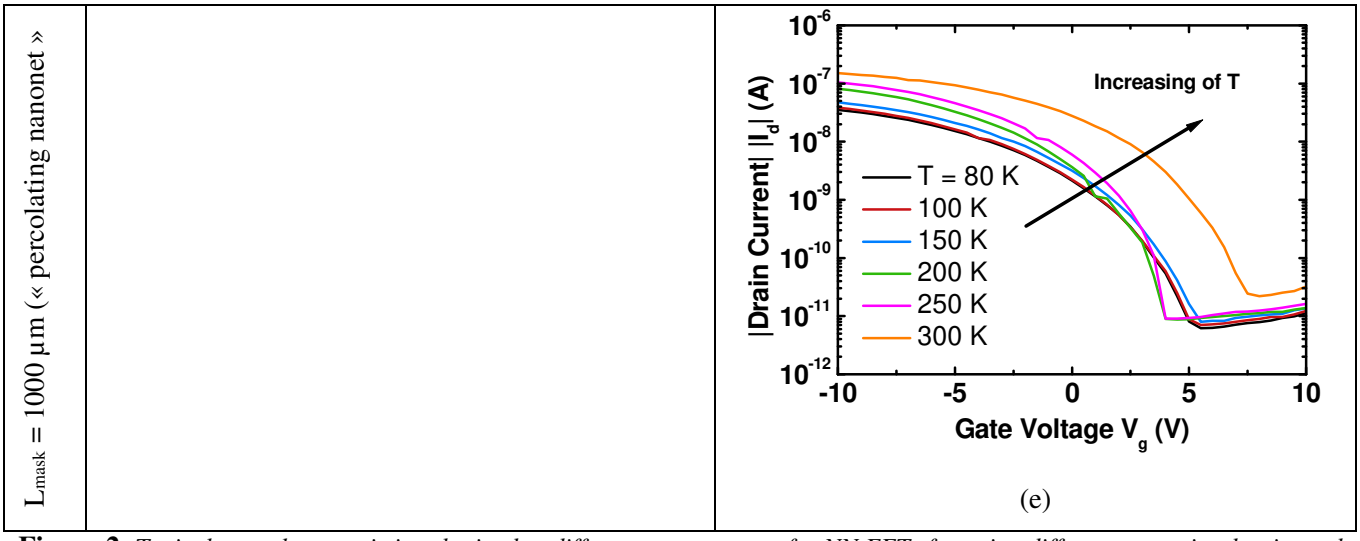


Figure 2. *Typical gate characteristics obtained at different temperatures for NN FETs featuring different nanowire density and channel length values. Nanowire density is equal to d_{Wires} = 0.28 NWs.µm^{-2} in the left hand side column and d_{Wires} = 0.65 NWs.µm^{-2} in the right hand side column. Channel length L_{mask} increases from 5 µm (1st line) to 50 µm (2nd line) and 1000 µm (3rd line). Drain voltage value is V_d = -4 V for d_{Wires} = 0.28 NWs.µm^{-2} and V_d = -9 V for d_{Wires} = 0.65 NWs.µm^{-2}.*

These curves were used to extract the main electrical parameters such as low field mobility μ_0, subthreshold slope ideality factor n and threshold voltage V_{th}. Extraction was performed in most cases by fitting the experimental curves with a Lambert $\mathcal{W}$ function.[27, 28, 29] In the few cases when the threshold voltage was out of the measurement window, we used instead a Y-function based model for μ_0 and V_{th} extraction. This was the case only for devices with 0.65 NWs.µm^{-2} and L_{mask} = 5 µm. The value of μ_0 was obtained using W_{mask} and L_{mask} as channel width and length, respectively. This provided an *apparent* low field mobility value suitable for compact modelling. Because physical width is smaller than W_{mask}, the extracted μ_0 is smaller than the physical mobility. This does not prevent variations to be analysed. Measurements were carried out on up to 5 devices of identical geometry for each value of L_{mask} and d_{Wires}. In the following, we will in general show the results obtained for these identical devices, in order to keep the information about variability.

4. DISCUSSION

A. Extraction of activation energy

In short channel devices (L_{mask} = 5 µm), conduction paths are mainly made of nanowires which connect directly source and drain. The temperature variation of mobility can thus be considered as indicative of transport mechanisms in the nanowires. In contrast, with channel lengths much longer than mean nanowire length (which is the case with

L_{mask} = 50 µm), current flows through a network of nanowires connected by inter-nanowire junctions. It is important to understand the role of these junctions in the percolating regime. This may allow getting some insight on their quality by proper analysis of experimental trends.

Fig.3 compares the temperature dependence of μ_0 obtained for L_{mask} = 5 µm and L_{mask} = 50 µm, for a NW density d_{Wires} = 0.28 NWs.µm^{-2}. For L_{mask} = 5 µm, μ_0 remained mostly constant or decreased slightly at low temperature, showing that the freezing of phonon scattering is screened and that scattering by defects is the prevailing scattering mechanism.[30] In contrast, it was observed that μ_0 decreased as temperature decreased for long channel devices (L_{mask} = 50 µm) operating in the percolating regime, with inter-nanowire junctions present along the conduction paths. This trend could in principle be consistent with the presence of energy barrier heights at the junctions and it is the aim of this paper to understand to which extent this is the case.

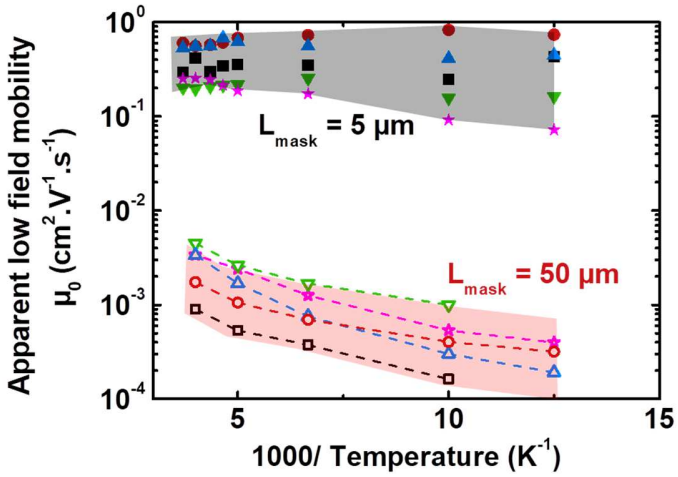


Figure 3. *Effective low field mobility as a function of temperature for a NW density of 0.28 NWs.µm^{-2}. Full symbols correspond to short devices (L_{mask} = 5 µm), while empty symbols correspond to long devices (L_{mask} = 50 µm).*

With a higher density of nanowires (d_{Wires} = 0.65 NWs.µm^{-2}) and short channel devices (L = 5 µm), similar temperature dependence of μ_0 was observed as μ_0 remained almost independent of temperature (plots obtained for L_{mask} = 5 µm in Fig.4). However this remained the case even with channels as long as 50 µm (plots for L_{mask} = 50 µm in Fig.4). Thermal activation was recovered only for much longer devices (as shown in Fig.5, with d_{Wires} = 0.65 NWs.µm^{-2} and L_{mask} = 1000 µm).

Altogether, the variation of μ_0 with temperature was more important when L_{mask} increased and d_{Wires} decreased.

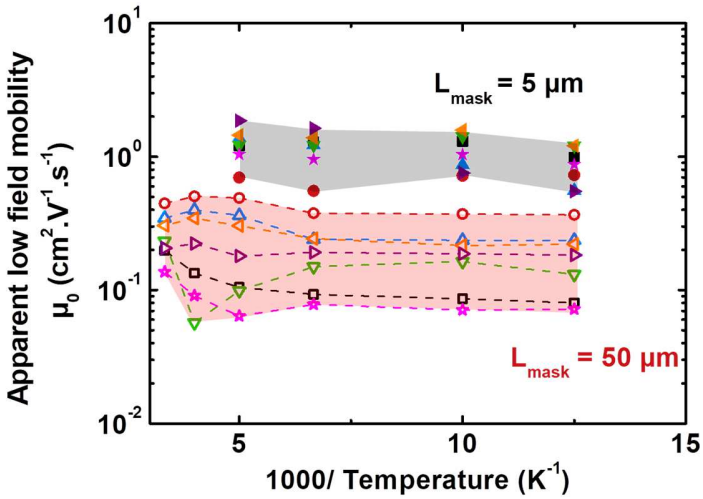


Figure 4. *Effective low field mobility as a function of temperature for a NW density of 0.65 NWs.μm^{-2}. Full symbols correspond to short devices (L_{mask} = 5 μm), while empty symbols correspond to long devices (L_{mask} = 50 μm).*

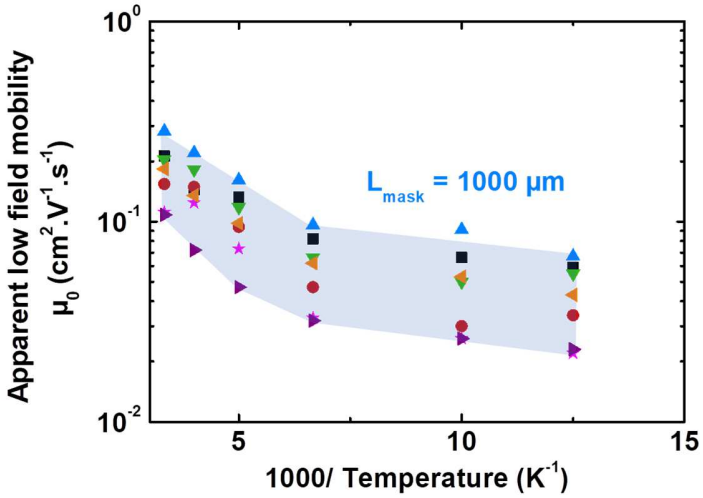


Figure 5. *Effective low field mobility as a function of temperature for a NW density of 0.65 NWs.μm^{-2}, and for a source-drain distance L_{mask} = 1000 μm.*

Fig.6 plots the temperature dependence of V_{th} for L_{mask} = 50 μm and two different values of density, with V_{th} becoming more positive with temperature increase.

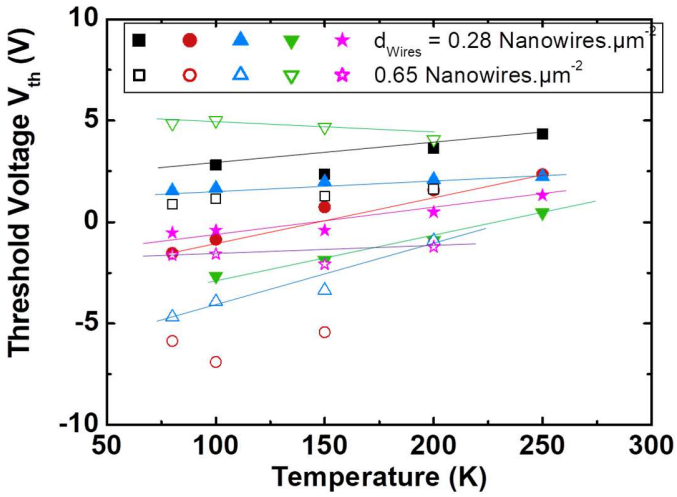


Figure 6. *Threshold Voltage V_{th} as a function of temperature for L_{mask} = 50 µm and two values of d_{Wires}. Filled symbols are for d_{Wires} = 0.28 nanowires.µm^{-2} and empty symbols are for d_{Wires} = 0.65 nanowires.µm^{-2}. The lines are only guides for the eyes.*

B. Extraction of the thermal activation energy of μ_0

We assumed that the difference in the temperature dependence of long channel devices, with respect to short channel devices, is related to the presence of inter-nanowire junctions along the channel. As a first approximation, the junctions were considered as potential barriers with height E_a, as usually done for grain boundaries.

A typical model for taking account of mobility temperature dependence, where current is controlled by a single barrier would be of the form:

$$\mu_0 = K \exp(- qE_a / k_bT) \qquad (1)$$

In this equation, K is a constant, k_b the Boltzmann constant, q the electron charge in absolute value and T the temperature. The thermal activation energy E_a (in eV) can be extracted from the slope of an Arrhenius plot of μ_0 (semi-log plot as a function of 1/T). To first order it is equal to the energy barrier height and provides thus a very interesting insight into the governing mechanisms of current conduction in the device.

Fig.7 shows the Arrhenius plot of μ_0 for one device with L_{mask} = 50 µm and d_{Wires} = 0.28 nanowires.µm^{-2}. From this plot, it is possible to extract a mean value of the activation energy E_{a_F}, describing the overall variation over the range of temperatures from 80 K to 200 K. For the device of Fig.7, E_{a_F} = 24 meV.

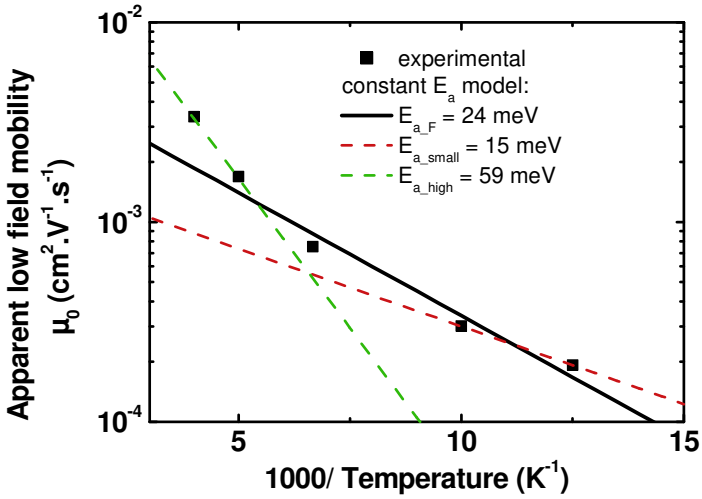


Figure 7. *μ_0 as a function of reciprocal temperature for one device with L_{mask} = 50 µm and d_{Wires} = 0.28 nanowires.µm^{-2}. Square symbols are for experimental data. Red line (resp. green line) are obtained by fit of experimental data with the equation (1) for the range of temperature from 80 K to 100 K (resp. 200 K to 250 K). Black line is obtained by a fit of experimental data with equation (1) for the range of temperatures from 80 K to 200 K.*

Fig.8 shows E_{a_F} as a function of d_{Wires} for different values of L_{mask}. E_{a_F} decreased with d_{Wires} and globally increased with L_{mask}.

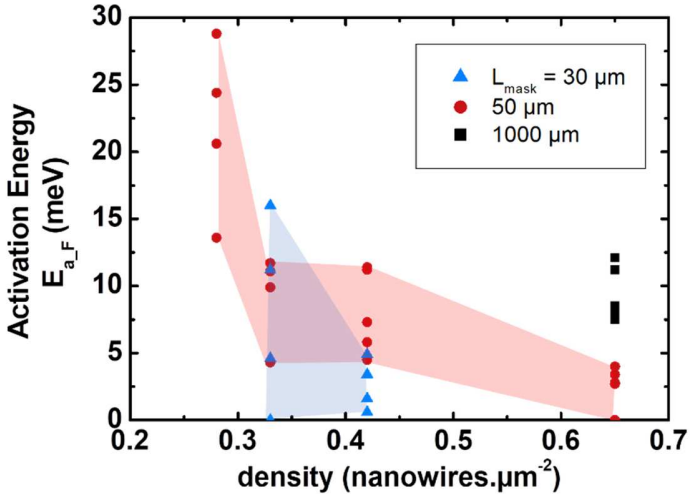


Figure 8. *Activation energy E_{a_F} function of the nanowire density for different values of L_{mask} (extracted as from solid line in Fig.7)*

However, the experimental Arrhenius plots did not show a linear trend on the whole range of temperatures. In the example of Fig.7, the activation energy extracted at low temperature is much lower than that extracted between 200 K and 250 K. To explain such a trend, it is necessary to assume that energy barrier height shows some variability from one junction to another.

C. Activation energy dispersion

Activation energy dispersion can be explained by local variability of junction sintering. The influence of dispersion has been tentatively explained in [31] with an ideal model made of an infinity of junctions in parallel with a Gaussian distribution for the energy barrier at individual junctions. However this model is not general, nor would be a model with only junctions in series, as a real nanonet normally involves a mixture of series and parallel paths. For qualitative analysis we will discuss E_{a_F} variations while full simulation will be provided in next section.

On Fig.8, E_{a_F} decreases with d_{Wires} and increases with L_{mask}. Fig.9-(a) shows an ideal case where electrons can only pass through one conduction path made of nanowires in series. This ideal case can be only obtained for a small d_{Wires} (or a long L_{mask}). If there is a dispersion of E_a for individual junctions, E_{a_path}, activation energy of the path, will be equal to the maximum of E_a involved in the path. If d_{Wires} increases (or L_{mask} decreases), parallel conduction paths will be formed between source and drain (Fig.9-(b)). In this case, activation energy of the nanonet can only decrease, if one of the parallel paths has an activation energy smaller than E_{a_path}.

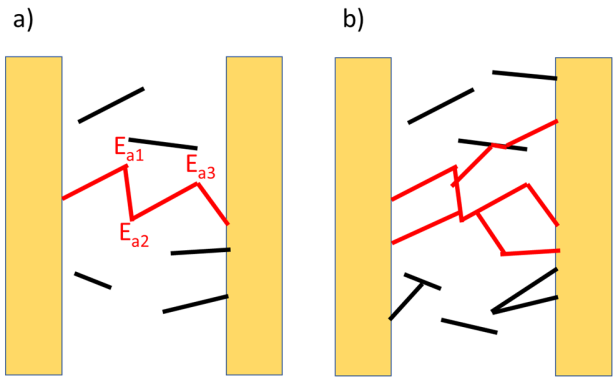


Figure 9. *a) Schematic of the ideal conduction path obtained for small d_{Wires}. In this case, activation energy of the path is the one of the junctions involved in the path with the higher value of activation energy. b) d_{Wires} increases. In this case, activation energy of the network can be only inferior to the one of the figure a). A decrease in L_{mask} has a similar effect, with the predominance of single conductive path for long L_{mask}, and of parallel paths for short L_{mask}.*

On Fig.6, V_{th} increases with temperature increase. For classical structure of FETs, this result is known and is linked to a variation of surface potential.[32] But this variation is not visible for devices with L_{mask} = 5 µm, so there is probably a supplementary contribution due to the junctions. Because of E_a dispersion for individual junctions, there is a variation of electrically active density with temperature (some insulating junctions becoming more conductive as temperature increases). Based on [18] it is known than an increase of the density will lead to a more positive V_{th}, if there is a

dispersion of V_{th} for individual nanowires. To summarize, an increase of the temperature will lead to an increase of the electrically active area, and thus to a more positive V_{th}.

In conclusion, taking account of an activation energy dispersion for individual junctions could explain the temperature dependence of μ_0 and V_{th} and the variations of E_{a_F} with d_{Wires} and L_{mask}. However there is no simple model to confirm this qualitative description. A Monte-Carlo simulation of NN FET mobility as a function of temperature was thus performed in order to evaluate the influence of junction barrier heights and of their dispersion.

D. NN FET mobility Monte Carlo simulation for different temperatures

This simulation was based on the temperature dependent model of nanowires and junctions, based on experimental results.

Junctions are considered as temperature dependent resistance, which vary following Equation (2):

$$G_{junction\_i} = G_0 \exp(-E_{a\_i} / k_bT) \qquad (2)$$

In this equation $G_{junction\_i}$ is the conductance of the junction i and E_{a_i} activation energy of the junction i. E_{a_i} will be randomly generated according to the chosen density of probability. The value of G_0 was chosen so as to have a good order of magnitude for junction resistance, close to 10 MΩ at 300 K. For simplicity, threshold voltage dispersion for individual nanowires is not taken in account in the model. For a chosen V_g, all the nanowires of the nanonet were considered to have the same conductivity, the temperature dependence of which was neglected based on the temperature dependence found in short channel devices ("nanowires in parallel" regime).

Several nanonet structures were built, for each geometry (given values of Source-Drain distance L_{mask} and pad width W_{mask}), by randomly generating a number N_{NW} of nanowires defined by the position of their centre (2D coordinates x_{0i} and y_{0i}) and their angle (θ_i) with respect to horizontal axis (taken along source-drain direction). The junctions between the nanowires were located. Then, a Kirchhoff matrix of conductance was filled, using the above mentioned models for nanowire segments and inter-nanowire junctions A similar matrix filling technique has been used for the study of junction dispersion and structural parameter influence on CNT-network conductance, however with a temperature independent purely resistive model for the junctions.[33] Finally, this matrix was used to obtain the NN FET conductivity between source and drain. The current was calculated for a large negative gate voltage (ON-current I_{on}).

Here, low field mobility is proportional to I_{on} since threshold voltage dispersion was neglected so that we will discuss indifferently I_{on} and μ_0 variations.[18] In the next part, different densities of probability were tested for activation energy dispersion.

1) Gaussian dispersion

As a first assumption, activation energy dispersion was modelled as a Gaussian distribution with a mean value E_{a0} and a standard deviation σ_{Ea}. Fig.10 shows the temperature dependence of I_{on} for L_{mask} = 30 µm and d_{Wires} = 0.13 NW.µm^{-2} and two Gaussian distribution functions, one with E_{a0} = 120 meV and σ_{Ea} = 40 meV and the other one with E_{a0} = 120 meV and σ_{Ea} = 20 meV.

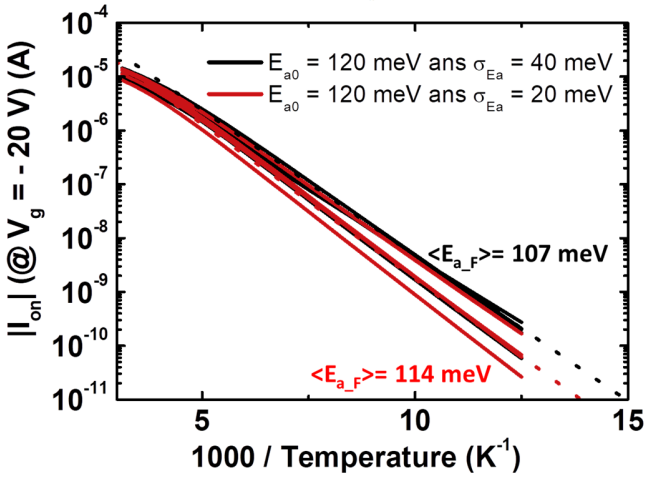


Figure 10. *I_{on} simulated value for V_g = -20 V function of the invert of the temperature for 2 different distributions of E_a (E_{a0} = 120 meV and σ_{Ea} = 40 meV in black and E_{a0} = 120 meV and σ_{Ea} = 20 meV in red), for L_{mask} = 30 µm and d_{Wires} = 0.13 nanowires.µm^{-2}. 5 realizations are plotted for each distribution. Dotted lines correspond to the linear fit mean values.*

For a Gaussian dispersion of activation energy, I_{on} varied linearly with the inverse of temperature. The extracted E_{a_F} was closed to E_{a0}. Increase of σ_{Ea} lead to a small decrease of E_{a_F}.

This figure does not fit the experimental data showed on Fig.7. This can be due to the characteristics of the Gaussian distribution. Indeed, to keep some physical meaning, it had to be truncated to zero. If the standard deviation is not small enough compared to the mean value, this process generates a large number of null barrier height values, which would drive the distribution far from a strictly speaking Gaussian one. It was thus necessary to keep σ_{Ea} small enough compared to E_{a0}. However, in this case, the amount of very small barrier heights is small and the chance to get a path that can

connect source and drain through such low barrier height junctions runs towards zero. This explains why the plateau at low temperature is not observed in the Arrhenius plot of I_d in the frame of this assumption.

2) Bimodal dispersion

In order to explain experimental results, we formulated another hypothesis, where activation energies would be distributed along a bimodal function, with 2 families of inter-nanowire junctions in the network. The presence of several families is not unconceivable as the quality of the sintering process may be non-uniform, depending on several parameters such as nanowire diameter, native oxide thickness and removal efficiency, among others. We retained the simplest picture where good sintering would be obtained in some places while a residual barrier would remain elsewhere.

In order to test this assumption against experimental trends, our Monte-Carlo simulations are now assuming that there is no energy barrier for a fraction of the inter-nanowire junctions while, for the remaining junctions, there is an energy barrier which follows a Gaussian law. The parameter P_0 refers to the fraction of junctions with a zero value of E_a. P_0 can vary between 0 % (all the junctions in the network have an activation energy which follows the Gaussian law) and 100 % (all energy barriers at inter-nanowire junctions are equal to 0 eV).

The operation mechanism is schematically described in Fig.11. In this figure, the black dots represent the junctions which feature an energy barrier. At low temperature, the conduction paths which involve these junctions are blocked and the only conducting paths are those which involve purely resistive junctions (no energy barrier). Current flows through the sub-network of nanowires connected by such junctions and a plateau with low activation energy is seen. If P_0 is too small or if the nanowire density is too low, there is a risk that this sub-network is below the percolation threshold and the low activation regime is not seen. At higher temperature, the other junctions start to be conductive and current can flow through the whole network, with a hierarchy of conducting paths which can be completely different from what it is at low temperature.

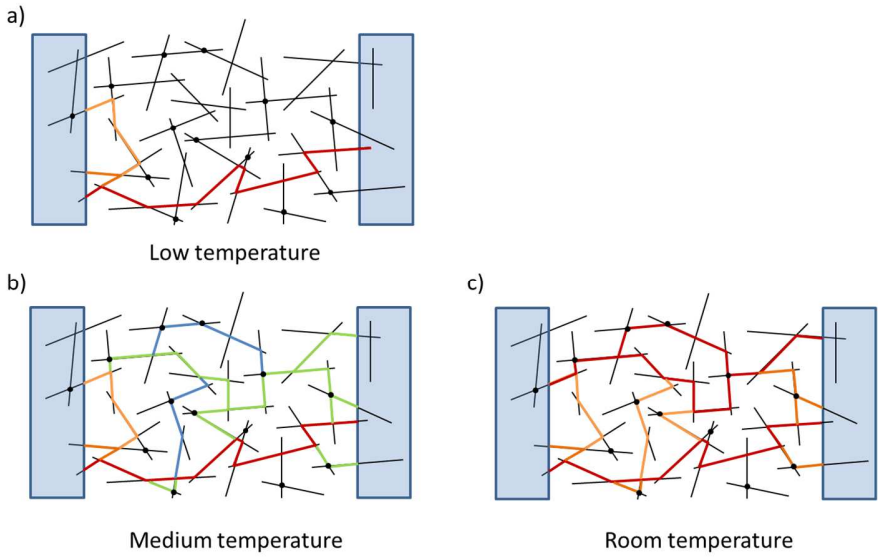


Figure 11. *Schematic representation of the conduction paths across an NN FET as a function of temperature under the assumption that there is an energy barrier at the interface of some of the inter-nanowire junctions (marked with black dots) while the other ones have no energy barrier. The red lines are conductive paths, black lines are insulating, blue and green lines are highly resistive paths. At low temperature, current can flow only through the small number of conductive paths that involve nanowires separated from each other by purely resistive junctions (no energy barrier). As temperature increases, the junctions with small values of E_a become more conductive and current can flow through additional paths that involve junctions with small and large values of E_a. There is an increase of the electrically active density of nanowires with the temperature, without a change of the physical density of nanowires.*

We started the analysis by studying the influence of P_0 on the temperature dependence of I_{on} (Figure 12). Five different random realizations were drawn by lot with the same channel length and nanowire density (L_{mask} = 30 µm and d_{Wires} = 0.13 nanowires.µm^{-2}). They are differentiated by curve colours in the plots of Figure 12. The parameters of the junctions were then chosen randomly, with several values of P_0 and the same Gaussian distribution for temperature activated junctions (E_{a0} = 60 meV and σ_{Ea} = 10 meV).

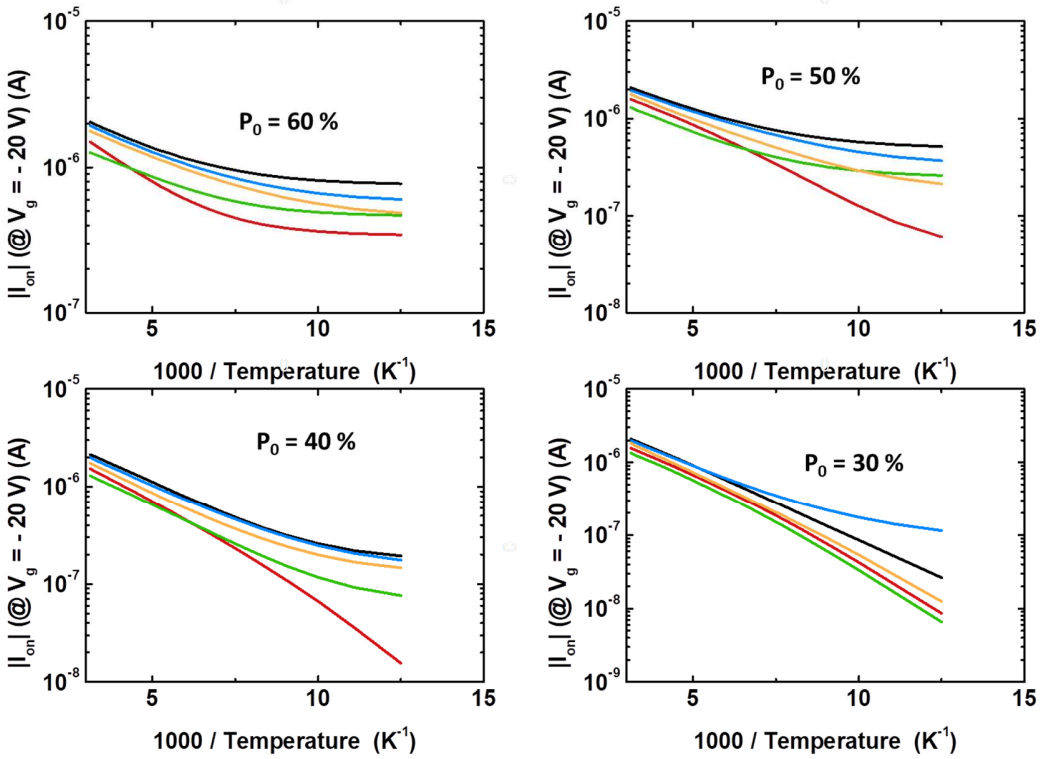


Figure 12. *I_d simulated value for V_g = -20 V function of the invert of the temperature for different values of P_0, a configuration L_{mask} = 30 µm and d_{Wires} = 0.13 nanowires.µm^{-2} and a chosen Gaussian Law with E_{a0} = 60 meV and σ_{Ea} = 10 meV. P_0 can vary between 0 % (all the junctions in the network have an activation energy which follows the Gaussian law) and 100 % (all energy barriers at inter-nanowire junctions are equal to 0 eV)*

For large P_0 values, simulated I_{on} versus 1/T curves follow the same qualitative behaviour as experimentally. At low temperature, the only conducting junctions are those with E_a = 0 eV and a plateau, corresponding to the conduction through non thermally activated junctions, becomes visible in the Arrhenius plot. When temperature increases, junctions with non-zero E_a values are activated, and the temperature dependence of I_{on} at room temperature is a combination of the temperature dependence of the two families of junctions. It should be noted that for small value of P_0, some I_{on} versus 1/T plots do not reach a plateau at low temperature. These behaviours can be explained by the fact than in such case, it may happen that there is no conduction path solely made of non-activated junctions. Then, even at low temperature, the temperature dependence of I_{on} is mainly driven by the junctions with high value of E_a.

It is then interesting to know if this model can provide the correct trends for the variation of the activation energy as a function L_{mask} and d_{Wires}. For this study, the activation energy was extracted as experimentally as the mean value within the range of temperatures from 80 K and 200 K and the parameters for E_a distribution was kept the same for the random generation of energy barriers at inter-nanowire junctions (P_0 = 50 %, E_{a0} = 60 meV and σ_{Ea} = 10 meV). P_0 is chosen equal

to 50 % in order to observe the influence of non activated junctions to the temperature dependence of I_{on}. Fig.13 shows E_{a_F} variation as a function of d_{Wires} for different L_{mask} values. E_{a_F} obtained by simulation decreases with d_{Wires} and increases with L_{mask} at large NW density, which is the trend observed experimentally.

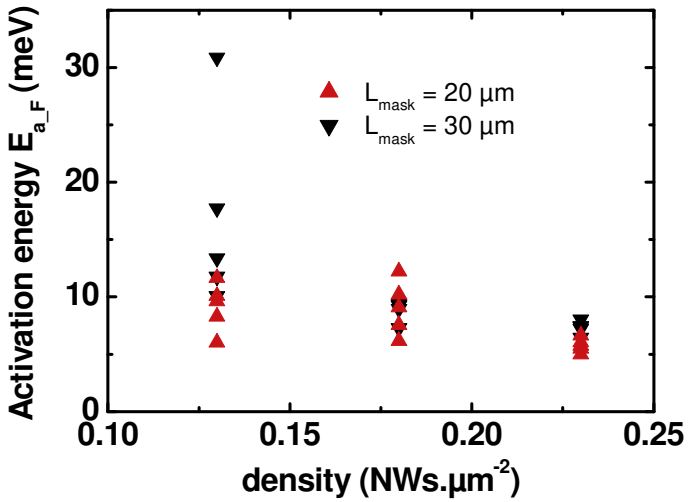


Figure 13. *E_{a_F} extracted from the simulation as a function of d_{Wires} and L_{mask} for P_0 = 50 %, E_{a0} = 60 meV and σ_{Ea} = 10 meV.*

5. CONCLUSIONS

We studied the evolution with temperature of the electrical characteristics of nanonet-based FET devices with different source-drain distances and nanowire densities. The analysis was supported by a modelling of carrier transport through a random network of nanowires. The role of inter-nanowires junctions was evidenced. In order to assess their influence on transport, a simple model, which assumed the presence of energy barriers at the junctions, was proposed. This model was updated, with an account for the dispersion of energy barriers values, so as to capture the distinctive features observed experimentally. It was then implemented within a Monte-Carlo description of the Si-NN. Comparison of simulation results with experimental trends steered the analysis towards a picture where a significant proportion of the junctions would be purely resistive, while the others would have an energy barrier. It is concluded that, with proper analysis of electrical characteristics dependence with temperature, source-drain distance and nanowire density, it is possible to get some insight, and thus to provide some technological feedback, about the role of inter-nanowire junction quality in nanonet-based devices.

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REFERENCES

[1] Cui Y, Wai Q, Park H, Lieber CM. Nanowire Nanosensors for Highly sensitive and selective detection of biological and chemical species. Sciences 2001; 293; pp.1289-1292. https://doi.org/10.1126/science.1062711

[2] Jayakumar G, Hellström PE, Östling M. Monolithic Wafer Scale Integration of Silicon Nanoribbon Sensors with CMOS for Lab-on-Chip Application. Micromachines 2018; 9; number 544. https://doi.org/10.3390/mi9110544

[3] Takato H, Sunouchi K, Okabe N, Nitayama A, Hieda K, Horiguchi F, Masuoka F. High performance CMOS surrounding-gate transistor (SGT) for ultra high density LSIs. Technical Digest., International Electron Devices Meeting 1988. https://doi.org/10.1109/IEDM.1988.32796

[4] Oh JY, Lee SM, Park JT, Triplett M, Yu D, Islam MS. Demonstration of gate-all-around FETs based on suspended CVD-grown silicon nanowires. 2013 IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S) 2013. https://doi.org/10.1109/S3S.2013.6716567

[5] Quitoriano NJ, Kamins TI. Integratable nanowire transistors. Nano Letters 2008; 8; 4410-4414. https://doi.org/10.1021/nl802292h

[6] Heo K, Cho E, Yang JE, Kim MH, Lee M, et al. Large-scale assembly of silicon nanowire network-based devices using conventional microfabrication facilities. Nano Letters 2008; 8; 4523–4527. https://doi.org/10.1021/nl802570m

[7] Gruner G. Carbon nanonets spark new electronics. Scientific American 2007; 296; 76–83. https://doi.org/10.1038/scientificamerican0907-48sp

[8] Snow ES, Novak JP, Campbell PM, Park D. Random networks of carbon nanotubes as an electronic material. Applied Physics Letters 2003; 82; 2145. https://doi.org/10.1063/1.1564291

[9] Kumar S, Murthy JY, Alam MA. Percolating Conduction in Finite Nanotube Networks. Physical Review Letters 2005; 95; 066802. https://doi.org/10.1103/PhysRevLett.95.066802

[10] Unalan HE, Zhang Y, Hiralal P, Dalal S, Chu D, Eda G, Teo KBK, Chhowalla M, et al. Zinc Oxide Nanowire Networks for Macroelectronic Devices. Applied Physics Letters 2009; 94; 163501. https://doi.org/10.1063/1.3120561

[11] Oueriemi I, Raskin JP, Choubani F, Huynen I. Wideband non-linear characteristics of random multi-walled carbon nanotubes network. Microwave and Optical Technology Letters 2013; 55; 2648-2652. https://doi.org/10.1002/mop.27842

[12] Joo MK, Mouis M, Jeon DY, Kim GT, Kim UJ, Ghibaudo G. Static and low frequency noise characterization of N-type random network of carbon nanotubes thin film transistors. Journal of Applied Physics 2013; 114; 154503. https://doi.org/10.1063/1.4825221

[13] Topinka MA, Rowell MW, Goldhaber-Gordon D, McGehee MD, Hecht DS, Gruner G. Charge Transport in Interpenetrating Networks of Semiconducting and Metallic Carbon Nanotubes. Nanoletters 2009; 9; 1866-1871. https://doi.org/10.1021/nl803849e

[14] Yanagi K, Udoguchi H, Sagitani S, Oshima Y, Takenobu T, Kataura H, Ishida T, Matsuda K, Maniwa Y. Transport mechanisms in metallic and semiconducting single-wall carbon nanotube networks. ACS Nano 2010; 4; 4027-4032. https://doi.org/10.1021/nn101177n

[15] Caicedo N, Leturcq R, Raskin JP, Flandre D, Lenoble D. Detection mechanism in highly sensitive ZnO nanowires network gas sensors. Sensors and Actuators B: Chemical 2019; 297; 126602. https://doi.org/10.1016/j.snb.2019.05.079

[16] Ternon C, Serre P, Lebrun JM, Brouzet V, Legallais M, et al. Low Temperature Processing to Form Oxidation Insensitive Electrical Contact at Silicon Nanowire/Nanowire Junctions. Advanced Electronic Materials 2015; 1; 1500172. https://doi.org/10.1002/aelm.201500172

[17] Legallais M, Nguyen TTT, Mouis M, Salem B, Ternon C. Toward the integration of Si nanonets into FETs for biosensing applications. Joint International EUROSOI Workshop and International Conference on Ultimate Integration on Silicon 2017. https://doi.org/10.1109/ULIS.2017.7962570

[18] Cazimajou T, Legallais M, Mouis M, Ternon C, Salem B, Ghibaudo G. Electrical characteristics of silicon percolating nanonet-based Field Effect Transistors in the presence of dispersion. Solid-State Electronics 2018; 143, 83-89. https://doi.org/10.1016/j.sse.2017.11.013

[19] Cazimajou T, Mouis M, Ghibaudo G. Finite element simulation of 2D percolating silicon-nanonet field-effect transistor. Joint International EUROSOI Workshop and International Conference on Ultimate Integration on Silicon 2018. https://doi.org/10.1109/ULIS.2018.8354760

[20] Cazimajou T, Theodorou C, Legallais M, Nguyen TTT, Mouis M, Ternon C, Salem B, Ghibaudo G. Low-frequency Noise Characterization of Si Nanonet Field Effect Transistors. International Conference on Noise and Fluctuations 2019. https://doi.org/10.5075/epfl-ICLAB-ICNF-269289

[21] Legallais M, Nguyen TTT, Mouis M, Salem B, Robin E, Chenevier P, Ternon C. An innovative large scale integration of silicon nanowire-based field effect transistors. Solid-State Electronics 2018; 143; 97-107. https://doi.org/10.1016/j.sse.2017.11.008

[22] Legallais M, Nguyen TTT, Cazimajou T, Mouis M, Salem B, Ternon C. Material engineering of percolating silicon nanowire networks for reliable and efficient electronic devices. Materials Chemistry and Physics 2019; 238; 121871. https://doi.org/10.1016/j.matchemphys.2019.121871

[23] Nguyen TTT, Cazimajou T, Legallais M, Arjmand T, Nguyen VH, Mouis M, Salem B, Robin E, Ternon C. Monolithic fabrication of nano-to-millimeter scale integrated transistors based on transparent and flexible silicon nanonets. Nano Futures 2019; 3; 2. https://doi.org/10.1088/2399-1984/ab1ebc

[24] Serre P, Ternon C, Stambouli V, Periwal P, Baron T. Fabrication of silicon nanowire networks for biological sensing. Sensors and Actuators B: Chemical 2013; 182; 390-395. https://doi.org/10.1016/j.snb.2013.03.022

[25] Mutiso RM, Sherrott MC, Rathmell AR, Wiley BJ, Winey KI. Integrating simulations and experiments to predict sheet resistance and optical transmittance in nanowire films for transparent conductors. ACS Nano 2013; 7; 7654–7663. https://doi.org/10.1021/nn403324t

[26] Stauffer D, Aharony A. Introduction to Percolation Theory. 1994

[27] Akkez IB, Cros A, Fenouillet-Beranger C, Boeuf F, Rafhay Q, Balestra F, Ghibaudo G. New parameter extraction method based on split C–V measurements in FDSOI MOSFETs. Solid-State Electronics 2013; 84; 142-146. https://doi.org/10.1016/j.sse.2013.02.011

[28] Karatsori TA, Theodorou CG, Ioannidis EG, Haendler S, Josse E, Dimitriadis CA, Ghibaudo G. Full gate voltage range Lambert-function based methodology for FDSOI MOSFET parameter extraction. Solid-State Electronics 2015; 11; 123-128. https://doi.org/10.1016/j.sse.2015.06.002

[29] Cazimajou T, Legallais M, Mouis M, Ternon C, Salem B, Ghibaudo G. Electrical characterization of percolating silicon nanonet FETs for sensing applications. Joint International EUROSOI Workshop and International Conference on Ultimate Integration on Silicon 2017. https://doi.org/10.1109/ULIS.2017.7962591

[30] Ando T, Fowler AB, Stern F. Electronic properties of two-dimensional systems. Reviews of Modern Physics 1982; 54; 437. https://doi.org/10.1103/RevModPhys.54.437

[31] Cazimajou T, Legallais M, Nguyen TTT, Mouis M, Ternon C, Salem B, Ghibaudo G. Low Temperature Electrical Characteristics of Si Nanonet Field Effect Transistors. Joint International EUROSOI Workshop and International Conference on Ultimate Integration on Silicon 2019.

[32] Jeon DY, Park SJ, Mouis M, Barraud S, Kim GT, Ghibaudo G. Low-temperature electrical characterization of junctionless transistors. Solid-State Electronics 2013; 80; 135-141. https://doi.org/10.1016/j.sse.2012.10.018

[33] Simoneau LP, Villeneuve J, Aguirre CM, Martel R, Desjardins P, Rochefort A. Influence of statistical distributions on the electrical properties of disordered and aligned carbon nanotube networks. Journal of Applied Physics 2013; 114; 114312. https://doi.org/10.1063/1.4821885