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Abstract

Motivated to produce reliable and performant SiNW-based transistors, we present in this work how percolating networks composed of randomly oriented SiNWs, called nanonets, are a promising material if they are well engineered. We demonstrate that a proper material engineering of nanonets via alumina encapsulation allows to drastically enhance the electrical characteristics of back gate field effect transistors (FETs). Based on a simple, low temperature (≤400°C) and up-scalable process of integration, the fabricated FETs exhibit a low off-current in the picoampere range while maintaining very good on-performance, up to the microampere and thus on-to-off ratio exceeding 10^5. As stated in this work, these nanonet-FETs present not only comparable electrical performances as reported single SiNW-based transistors in the same geometry but also good device-to-device reproducibility. This initial benchmarking clearly indicates that Si nanonet-based devices display essential features in terms of performances and fabrication process for sensing and flexible electronics.

Keywords:

Silicon nanowire, percolating network, field effect transistor, alumina encapsulation, electrical characterizations

1 Introduction

In the past two decades, one-dimensional nanostructures[1] have emerged as promising candidates for a new class of electronic devices able to meet the "More Than Moore" demand.[2]. This approach,[3] in opposition with the down-scaling drawing by the Moore's law[4], consists in adding new features and functionalities to microelectronic chips by using not only different integration schemes but also by exploiting nanomaterials. Indeed, due to their high surface-to-volume ratio, these nanostructures are featuring novel interesting properties which broaden their range of applications, especially in the fields of optoelectronics, energy and sensing.[1,5] It therefore requires the development of interfaces to connect the nanoscale components to the macroscopic world, without the need for complex technological processes and tools poorly compatible with the standard microelectronic technology.

Since their first integration into transistor by Lieber's group in 2000,[6] interest of single silicon nanowire (SiNW)-based devices is an evidence and silicon nanowires (SiNWs) have been among the most studied 1D nanostructures.[7,8] They have been successfully used as building blocks to fabricate various devices such as field effect transistors,[6,9–15] diodes,[16] bipolar transistors,[16] logic gates[17] and biosensors.[18–22] Basically, two different approaches[21–23] called top-down and bottom-up were developed to produce SiNW-based devices. On the one hand, top-down integration takes advantage of the well-established Complementary-Metal-Oxide-Semiconductor (CMOS) technology, but at the nanoscale, the integration process involves a succession of several complex or costly processing steps.[21] On the other hand, the development of the bottom-up approach is hampered by the lack of reliable methods to integrate SiNWs into functional devices at large scale. Various techniques reviewed by Noor and

Krull[21] have been investigated to align bottom-up SiNWs in a specially-defined manner and facilitate their integration. Whether the contacts are aligned to SiNWs or SiNWs are aligned between the contacts, it is extremely difficult to ensure that SiNWs will bridge the contacts and to properly control their numbers. Besides, device-to-device reproducibility directly suffers from process-induced variability of doping level or SiNW diameter and length.

Although important progress has been achieved to integrate SiNWs using both approaches, there remains challenges, not only in the development of a cost-effective, low temperature and flexible process but also in the production of reliable and reproducible devices over large areas.[22]

Percolating randomly oriented nanostructure networks, also called nanonets,[24] are a promising alternative since they benefit from bottom-up growth advantages while overcoming complex engineering integration of single SiNW. Moreover, they also offer additional interesting features. Firstly, there are methods to produce homogeneous nanonets over large areas with accurate control of nanostructure density.[25–30] At the same time, since nano-objects are handled collectively, their transfer onto the desired substrates, and thereby their further integration into functional devices, are greatly facilitated.[31,32] Secondly, due to the large number of nanostructures involved, nanonets possess the capability to smoothen nanowires variability by an averaging effect, making them highly reproducible and fault tolerant.[24,33] Up to date, despite the good potential of individual SiNW, their use in the form of nanonets for electronic device integration has been under-investigated,[33–36] likely due to the complexity to electrically stabilize the whole network.[34]

On the basis of our recently published proof-of-concept,[31] we report in this paper an efficient material engineering method to fabricate reproducible and

outstanding silicon nanonet-based field effect transistors. Our previous works had enhanced the role of junction sintering[37] and of silicide formation[31] at contacts. This work presents a step forward in the significant enhancement of transistor electrical properties via proper alumina encapsulation of nanonets. As a consequence their electrical performances can compete with those reported for single SiNW-based devices fabricated with bottom-up approach and similar back-gate configuration. Using only standard microelectronic techniques, our low temperature process (≤ 400°C) bypasses the issues of those currently used in the literature while being compatible with mass production. We believe these major technological breakthroughs broaden SiNW-based electronic applications. Indeed, in the competitive context of the More-Than-Moore race, our silicon nanonet FETs may be integrated into ultrasensitive biosensors as already reported for single SiNW-based devices or used as a building block for transparent flexible electronics thanks to transparency and the high mechanical flexibility of nanonets.[24]

2 Experimental section

2.1 Device fabrication

The fabrication of silicon nanonet bottom-gate field effect transistors combines a bottom-up approach for the nanonet fabrication and standard optical photolithography techniques for their integration as previously reported.[31] The collective handling of a large amount of SiNWs facilitates significantly their integration into transistors while the developed process is compatible with mass production and fulfill the temperature requirements for CMOS circuit. The whole fabrication process consists of seven main steps as depicted in **Figure 1**: (i) SiNW growth, (ii)fabrication and transfer of nanonets onto the substrate, (iii) SiNW-

SiNW junction sintering, (iv) alumina encapsulation, (v) contact fabrication, (vi) lift-off and (vii) silicidation.

(i) Silicon nanowires (SiNWs) were <111> vertically grown by the Vapor-Liquid-Solid-Chemical Vapour Deposition (VLS-CVD)[38] method using a dewetted gold thin films as catalyst and silane as precursor without adding doping gas. In these growth conditions, SiNWs are P-doped with a doping level in the range of 10^{16} cm^{-3}. Following the growth, gold catalyst was removed with a sequence of hydrofluoric acid treatment (HF) followed by gold etchant (KI-I_2 based solution). Afterwards, as-synthesized nanowires were dispersed in deionized water by sonication for 5 minutes and then the concentration of SiNWs was monitored by absorption spectroscopy, allowing the formation of highly reproducible SiNW suspension.[33]

(ii) 10 mL of the colloidal suspension was filtered through a nitrocellulose membrane in order to form randomly oriented SiNW network on the top of the filter.[33] Finally, the nanonet was transferred onto the desired substrate by membrane dissolution in acetone for 35 min. In order to achieve field effect transistors configured with a bottom gate, the substrate was constituted by a layer of 200-nm thick silicon nitride deposited onto heavily doped silicon wafer, corresponding to the gate dielectric and the gate respectively.

(iii) Sintering of SiNW-SiNW junctions was realized at low temperature via the process described elsewhere.[37] To do so, native silicon dioxide was first removed by HF-based treatment and then samples were annealed for 1 minute in nitrogen at 400°C.

(iv) Another HF-based treatment was performed before alumina atomic layer deposition using Fiji F200 Cambridge Nanotech apparatus. Al_2O_3 was deposited

at 250°C with trimethylaluminum and water as precursors. At a pressure of about 200 mTorr, 10 cycles were required to produce 1-nm thick layer of alumina.

(v) In order to pattern the future source-drain electrical contacts into the photoresist, photolithography technique (Süss Microtec MJB3 apparatus) was used. It is worth mentioning that only standard optical lithography apparatus are required. Moreover, this step does not necessitate any lithography alignments regarding the SiNW locations as SiNWs are homogeneously spread and form a kind of "thin film" (Figure 1(v)). Then, HF-based treatment was performed in order to remove alumina in the photoresist openings. Right after, 100 nm of nickel followed by 50 nm of gold were e-beam evaporated.

(vi) To reveal the contacts, the surplus of metal was lifted in AZ 100 remover.

(vii) Finally, a last thermal annealing was realized at 400°C in nitrogen in order to promote the formation of silicides and improve the electrical contact between the metal and SiNWs.

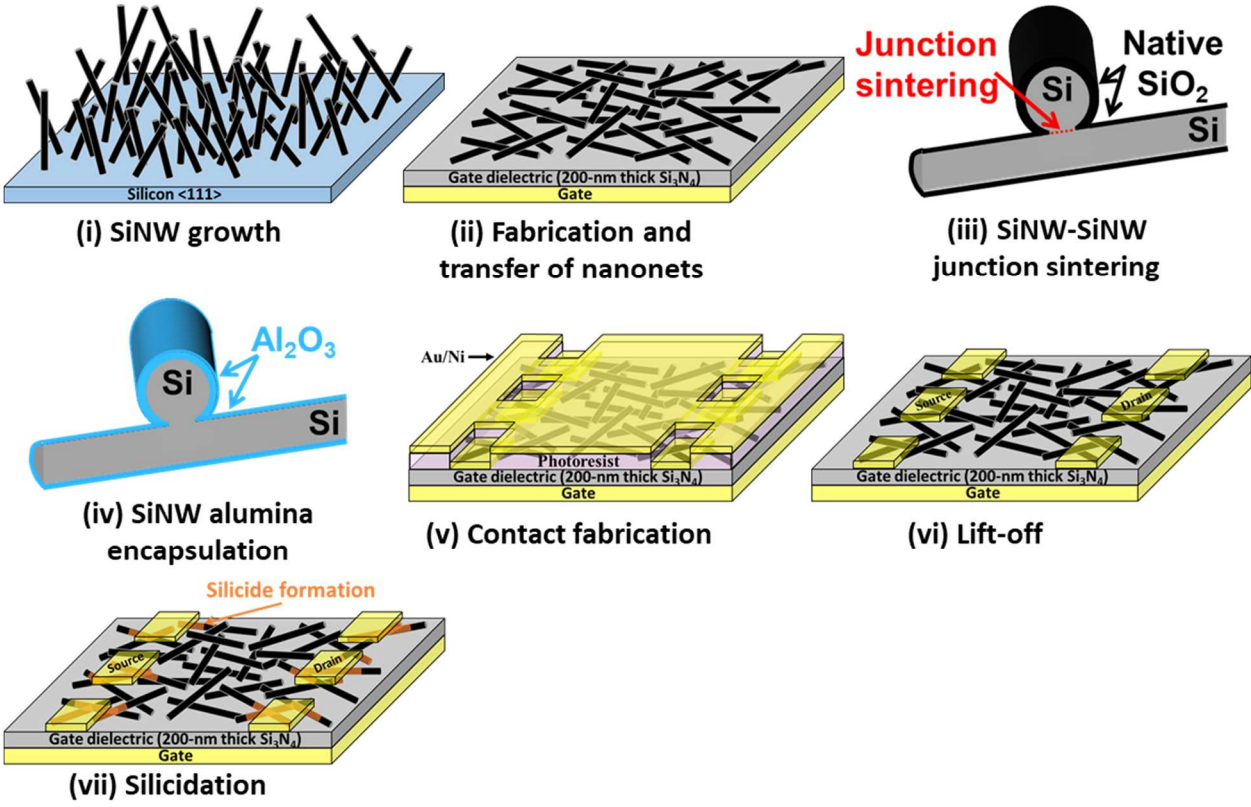

Fig. 1 Schematic representation of the seven main fabrication steps of the silicon nanonet bottom-gate field effect transistors: (i) SiNW growth, (ii) fabrication and transfer of nanonets onto the substrate, (iii) SiNW-SiNW junction sintering, (iv) alumina encapsulation, (v) contact fabrication, (vi) lift-off and (vii) silicidation.

2.2 Morphological characterizations

Si nanonets and devices were characterized by scanning electron microscope (SEM) using Hitachi S4100. SEM images were analyzed with ImageJ software. The SiNW density in nanonets was estimated by calculating the ratio between the percentage of SiNWs covering the substrate and the surface covered by each nanowire, considering the average diameter and length of SiNWs. In nanonets, the mean length and diameter of SiNWs is about $L_{SiNWs} = 6.9\ \mu m$ and $D_{SiNWs} = 39\ nm$, with a standard deviation of $2.8\ \mu m$ and $7\ nm$, respectively (see Figure S1 from Electronic Supplementary Material for details). All nanonets studied in this article present similar density of 23 x 10^6 NWs.cm^{-2}. The channel length corresponds to the distance between the contacts whereas the channel width is constant (200 µm).

2.3 Electrical characterizations

Two-probe Karl Süss station controlled by a HP4155A parameter analyzer was used for the electrical characterizations. These measurements were carried out in a dark environment and at room temperature. Transfer characteristics were swept from positive to negative gate voltages with a drain voltage of -4V, taken in the linear working regime (see Figure S2 from Electronic Supplementary Material for details). As reported previously for native SiO_2 Si-NNs, transistors display p-type operation and work on accumulation regime in the On state.[31]

3 Results and discussion

3.1 Encapsulation challenges for the future integration into transistor

The quality of the interfaces surrounding the channel is a key parameter for any field-effect transistors (FET) as it influences many parameters, from transconductance to low frequency noise[39,40]. In this work, the channel of the developed transistor was a P-type silicon nanonet (Si-NN). The channel length was longer than mean nanowire length. As a consequence, charge carriers flowing from source to drain had to cross several SiNW-SiNW junctions. The developed devices featured a back-gate configuration, where the substrate was used as the gate and the gate dielectric was a 200-nm thick silicon nitride (Si_3N_4) layer, as shown in **Figure 2**. In our previously reported Si-NN FETs,[31] the nanonet was surrounded by the native silicon dioxide layer which systematically grows, through a self-limited process, at the surface of silicon when stored in air.[37] It is known that this native SiO_2 provides poor-quality interfaces.[41] Its replacement by an encapsulation layer was thus considered essential to prevent silicon oxidation in air and to enhance Si-NN FETs electrical properties. A critical issue for the encapsulation of such a SiNW network is the preservation of the SiNW-SiNW junction sintering which is a key-step of the integration process as described in the method section. Such sintering step, that turns the assembly of SiNWs into a Si-nano-polycrystalline network, is essential to allow electrical conduction in long channel Si-NN FETs,[37] which involve more than one NW-NW junction in a conducting path (Figure 2).

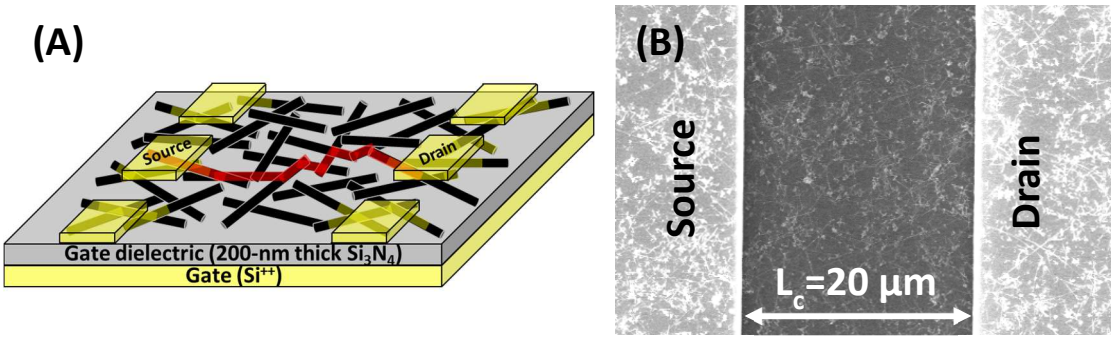

Fig. 2 Si nanonet-based field effect transistor (Si-NN FET) with a bottom gate configuration. (A) Scheme of Si-NN FET. One example of conducting path is highlighted in red for illustration. (B) SEM top-view of Si-NN FET with a channel length (L_c) of 20 µm.

Here, on the basis of the literature,[42–44] we opted for an alumina encapsulation layer as it is fully compatible with our integration process. It can be easily etched before contact deposition, using hydrofluoric acid (HF) treatments,[45] which induce no irreversible damages to the Si nanonet. Atomic Layer Deposition (ALD) was chosen for alumina deposition since it involves a self-limiting growth mechanism which enables the formation of high quality and homogenous thin films. Moreover, this technique provides a conformal coating and properly encapsulates SiNWs while preserving the sintered NW-NW junctions (**Figure 3**). The alumina thickness was varied from 2 nm to 8 nm to avoid excessive planarization of the top surface and to preserve the high surface-to-volume ratio, which is an essential morphological feature at the basis of SiNW remarkable properties.[13,46–48]

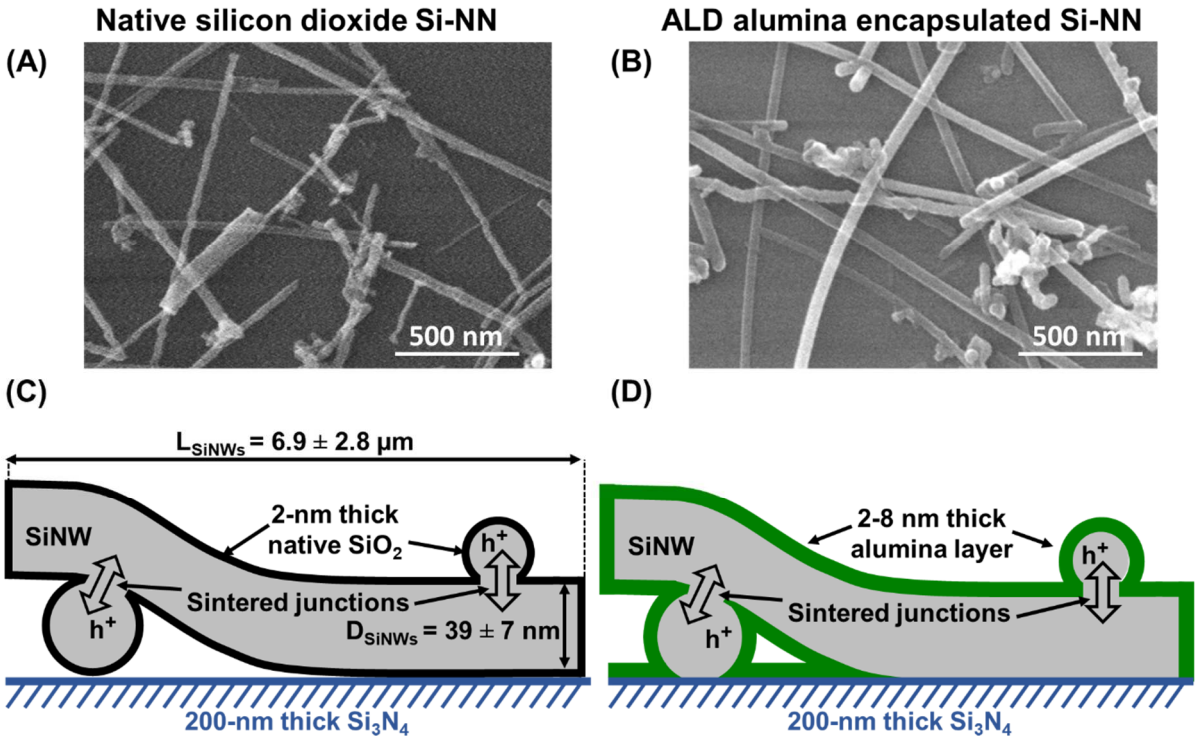

Fig. 3 Comparison between sintered Si-NN coated by (A, C) natively grown silicon dioxide and encapsulated by (B, D) alumina deposited using ALD. (A, B) refers to top-view SEM images of nanonets while (C, D) are cross-sectional schemes of 3 coated SiNWs: 1 sectioned in the length and 2 according to the diameter. For (C), the mean and standard deviation of SiNW length (L_{SiNWs}) and diameter (D_{SiNWs}) are indicated. For (D), due to conformal coating with ALD, alumina is deposited simultaneously on SiNWs and onto the substrate whereas SiNW-SiNW junctions and underneath SiNW portions are considered alumina-free.

3.2 Effect of alumina encapsulation on transistor electrical properties

We firstly investigated the effect of alumina encapsulation on FET electrical performance. To do so, we compared two transistors with similar channel length of 20 µm (such as the one shown in Figure 2(B)) but with different layers surrounding nanonets. One nanonet was encapsulated with 8 nm of alumina (Figure 3(B) and (D)) whereas the other one was covered by the 2 nm-thick native silicon dioxide[37] grown in air (Figure 3(A) and (C)). The transfer characteristics (drain current versus gate voltage at given drain voltage) are compared in **Figure 4**.

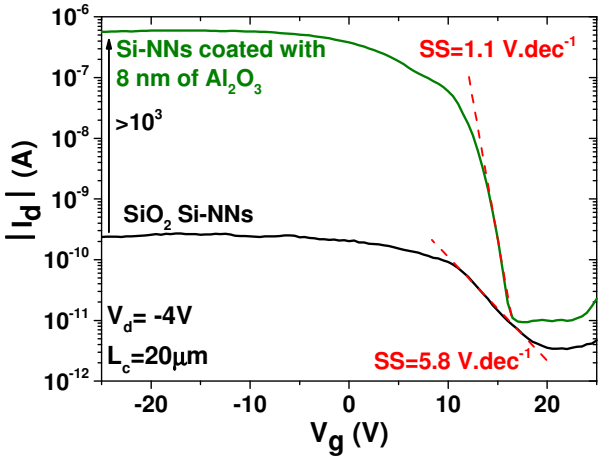

Fig. 4 Transfer characteristic comparison between devices constituted by either native 2 nm-SiO_2 Si-NN or 8-nm alumina coated Si-NN. For both, the channel length (L_c) is 20 µm and the drain voltage (V_d) was set at -4V.

One can immediately notice a drastic improvement of electrical performance with alumina encapsulation. Indeed, I_{On} increases by more than 3 orders of magnitude and the subthreshold slope decreases significantly from 5.8V.dec^{-1} for native-oxide Si-NN to 1.1V.dec^{-1} for alumina encapsulated Si-NN. Both nanonets were sintered in the same conditions, so that we can exclude a difference in the contribution of SiNW-SiNW junctions. The strong improvement of the subthreshold slope (SS) can be attributed to a reduction of the interface trap density which can be expressed as Equation 1.[49–51]

$$D_{it} \approx \left(\frac{SS \times e}{kT \ln 10} - 1\right)\frac{C_{ox}}{e} \qquad (1)$$

where k_B is the Boltzmann constant ($1{,}38 \times 10^{-23}\ J.K^{-1}$), C_{ox} is the gate capacitance, T refers to the temperature ($300\ K$) and e corresponds to the elementary charge ($1{,}6 \times 10^{-19}\ C$). According to the literature,[52,53] the gate coupling capacitance of nanonet transistors depends not only on the gate dielectric characteristics but also on the nanonet morphology. Considering the relative high SiNW density of the nanonets used in this study ($23 \times 10^6\ NWs.cm^{-2}$) and the

thick gate dielectric ($t_{ox} = 200\ nm$), the capacitance per unit area can be considered as a thin film standard plate capacitor defined as $C_{ox} = \varepsilon_0 \varepsilon_r / t_{ox}$ where ε_0 and ε_r represent the free space and dielectric permittivity, respectively. The capacitance per unit area was thereby assessed at $C_{ox} = 33\ nF.cm^{-2}$. Despite its overestimation for networks, this assumed capacitance can allow the comparison of the interface trap density[51] between native-oxide and encapsulated alumina Si NN-FETs. From the experimental results (Figure 4), D_{it} was estimated at $2 \times 10^{13}\ cm^{-2}.\ eV^{-1}$ and $4 \times 10^{12}\ cm^{-2}.\ eV^{-1}$ for Si-NN with native-oxide and those encapsulated with $8\ nm$ of alumina, respectively. This discrepancy clearly highlights that native SiO_2/SiNW interface is poor compared to alumina/SiNW interface. Indeed, the non-intentionally growth of native SiO_2 in air induces the formation of a high density of dangling bonds at the interface. Each interruption in the periodic lattice structure acts as an interface trap of carriers. These traps are thus responsible of the subthreshold slope degradation (Figure 4), and more generally, of the reduction of transistor performances.[54] On the contrary, alumina was grown via the well-controlled ALD process. Therefore, it allows the formation of a better interface quality and enhances the electrical characteristics. It is particularly remarkable that, for alumina encapsulated Si-NN FETs, I_{On} increases by more than 3 orders of magnitude while the Off current, measured at $V_g = 25V$, remains stable. This lead to a significant improvement in I_{On}/I_{Off} from 50 for native-oxide Si-NN to 2×10^4 for alumina encapsulated Si-NN. The large trap density at the interface between native SiO_2 and SiNWs is also responsible of an important degradation of carrier mobility in our Si-NN FETs.

3.3 Role of alumina thickness

To examine in details how alumina affected the electrical performances, two key parameters, the On current (I_{On}) and the subthreshold slope (SS), were statistically studied for various alumina thicknesses, ranging from $2\ nm$ to $8\ nm$. Native-oxide nanonets will be referred to as coated with $0\ nm$ of alumina. For each thickness, the electrical parameters from 7 to 28 measured transistors were extracted. The box charts of I_{On} and SS for each alumina thickness are shown in **Figure 5**(A) and (B). One can notice a significant improvement of both parameters, an increase of 4 orders of magnitude for I_{On} and a decrease of a factor 2,5 for SS, when the thickness of alumina increases from 0 to $8\ nm$. Interestingly, these two parameters tend to level off for an alumina thickness larger than $6\ nm$ along with a remarkable diminution of their dispersion. On one hand, these substantial enhancements confirm that alumina reduces drastically the interface trap density. On the other hand, an alumina thickness in the range of $6\ nm$ to $8\ nm$ is necessary to level off the electrical properties of Si-NN FETs.

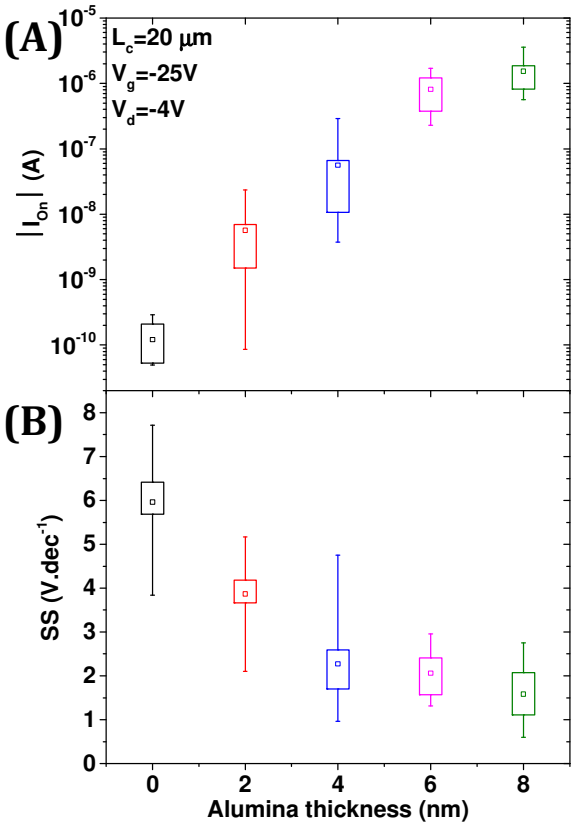

Fig. 5 Effect of the alumina thickness on the On current (I_{On}), extracted at -25V, and the subthreshold slope (SS). 0 nm of alumina corresponds to 2-nm thick layer of native SiO_2. For all transistors, the channel length (L_c) is 20 µm and the drain voltage (V_d) was set at -4V. The boxes show the 25th and 75th percentiles whereas the whiskers represents the 5th and 95th percentiles. The empty square in the boxes shows the mean value.

3.4 Electrical variability of silicon nanonet transistors

To assess thoroughly the electrical variability of Si NN-FETs, we extracted, in **Figure 6**, the On and Off current values for 65 transistors in total constituted by either native SiO_2 Si-NNs or 8-nm alumina coated Si-NNs with a channel length of 20 µm and 30 µm.

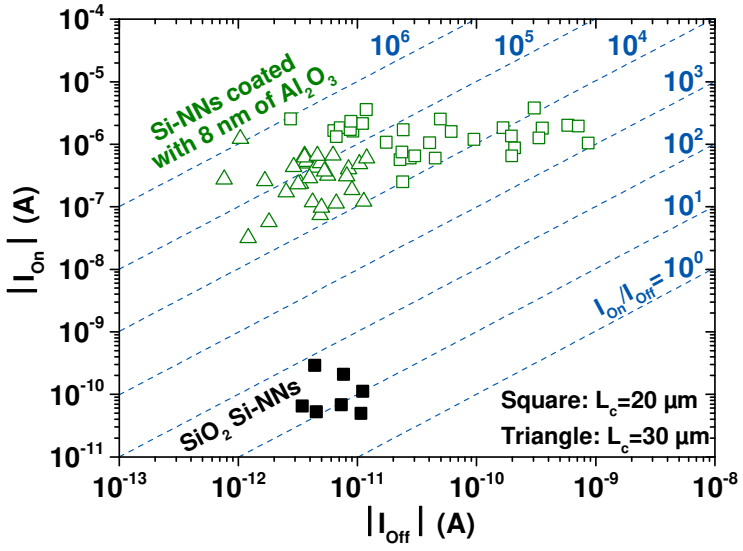

Fig. 6 Reproducibility of the On and Off current for transistors based on native SiO_2 Si-NNs (full symbol) and 8-nm alumina encapsulated Si-NNs (empty symbol) for 20 µm (square) and 30 µm (triangle) long channel. For native SiO_2 Si-NN based devices, no current is observed when channel length is 30 µm. The On-to-Off ratio (I_{On}/I_{Off}) is indicated by the dashed line. I_{On} and I_{Off} were extracted à -25V and +25V, respectively.

Firstly, for 20 µm-long channel, On current exhibits a systematic and significant increase of 4 orders of magnitude for alumina encapsulated Si-NNs compared to native SiO_2 Si-NNs FETs. This enhancement induces a simultaneous increase of the On-to-Off ratio which can reach outstanding values as high as 10^6. Nevertheless, despite a reproducible On current in the microampere range, one can notice an important dispersion of the On-to-Off ratio due to a variation of the Off current from $10^{-12}\ A$ to $10^{-9}\ A$. This observation may be attributed to the strong dispersion of SiNW diameter (from 25 nm to 60 nm) which induces a wide threshold voltage dispersion and thereby important modifications of electrical characteristics as previously simulated.[55]

Secondly, when increasing the channel length from 20 μm to 30 μm, we can observe a substantial reduction of the Off current and its further stabilization in the picoampere range. This improvement when increasing the channel length is

related to the nanonet's ability to "smooth disparities".[24,33] As more nanowires are involved in each conduction path, by an averaging effect, the important morphological differences no longer affect the electronic properties. Such averaging effect, demonstrated here statistically for the first time, is one of the advantages of nanonet-based devices over single nanowire ones whose electrical properties inevitably fluctuate with the nanowire morphological properties.[33] Thirdly, even though On current is expected to decrease when increasing the channel from 20 µm to 30 µm as standard thin film transistor, the diminution is still moderated which is in agreement with reported works on carbon nanotube nanonet-based transistors.[56,57] By combining the averaging effect of the nanonet through the long channel structure with the efficient sintering process, it is possible to level off both On and Off currents. As a consequence, highly reproducible SiNW-based FETs with On-Off ratio close to 10^5 were produced for 30 µm-long channel and Si-NNs encapsulated by 8-nm of alumina.

3.5 Benchmarking of silicon nanonet transistors

To highlight the performances of Si-NN FETs developed during this work and presented in this paper, a fair comparison with performances reported in the literature should be addressed. However, to our knowledge, because of systematic formation of SiNW-SiNW insulating junctions without the adequate sintering processing developed by our group, long channel Si-NN FETs are absent from the literature. As a consequence, this impedes us to make such an evaluation with similar devices. Therefore, the Si-NN FET benchmarking was realized through a comparison with single SiNW-based FETs that provide a baseline for expected performances in the targeted fields of application. Two criteria were taken into account: (i) SiNWs synthesized with a bottom-up method and (ii) integration of

single SiNW into FET with a bottom-gate configuration. Nanonet-based devices can thus be compared with devices made of nanostructures fabricated with similar synthesis processes but whose integration process is totally different. Merits and demerits of the nanonet device comparing with single nanowire FET are summarized in Table 1. Indeed, the Si-NN integration process that we have developed requires only standard optical lithography apparatus and does not require any lithography alignments regarding the SiNW locations (Figure 1(v)), making this method fully up-scalable and compatible with mass production. On the contrary, single SiNW-based transistor fabrication requires to localize and properly position the lithography setup regarding the SiNW location. This complex process cannot obviously lead to a high integration throughput and may even lead to defective devices due to misalignments. Unlike this integration of unique nanowires, it should be noted that the reliability of the process developed in this study for nanonet integration is exceptional. Indeed, for the Si-NNs, 100% of the devices measured were functional. The fault tolerance capability of Si-NNs allows to ensure the device functionality and even prevent the unexpected degradation of some percolating paths thanks to many others involved in the conduction.

The On-to-Off ratio and the subthreshold slope, key parameters related to transistor performances, were compared in **Figure 7**(A) and (B) as a function of channel length. It is remarkable that Si NN-FETs achieve On-to-Off ratios and subthreshold slopes as good as those reported for single SiNW devices. As the latter has proved their potential as excellent transistors[9] and even ultrasensitive biosensors,[18,19] these comparable electrical performances with one-decade longer transistors are completely promising for the future of Si-NN FETs. In the view of “More-than-Moore” approach, we believe that these major technological

breakthroughs open a broad range of applications. Indeed, in addition to bypass the complex engineering integration of SiNWs, our technology will take advantage to both the remarkable nanoscale component properties and reliable technological method to connect SiNWs with macroscopic world. In addition, given the outstanding characteristics of nanonets such as high reproducibility, mechanical flexibility and optical transparency, our Si-NN FETs fulfill essential characteristics for sensing applications and flexible electronics[58].

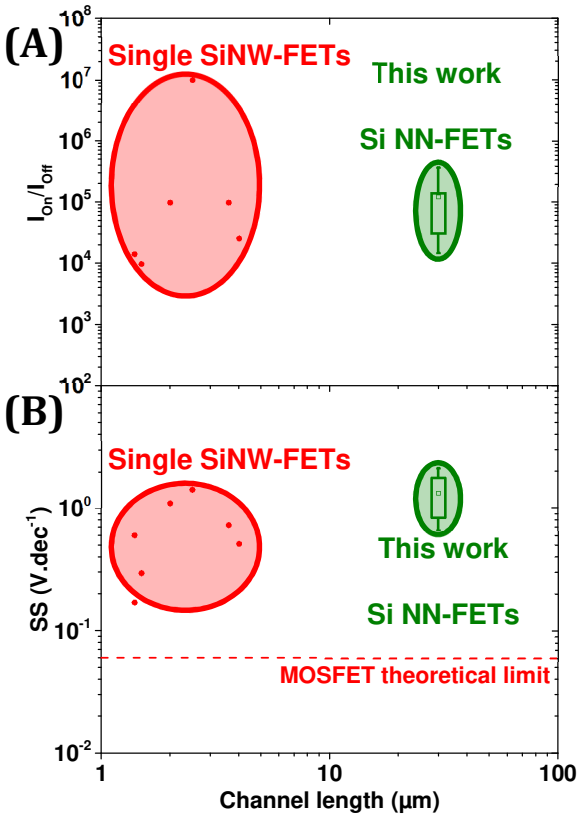

Fig. 7 Comparison of electrical performances between 8-nm alumina encapsulated Si NN-FETs (from this work) and single SiNW-FETs with a bottom-up approach and a bottom-gate configuration as reported in the literature[9,11,41,59–61]. (A) On-to-Off ratio (I_{On}/I_{Off}) and (B) subthreshold slope (SS) as a function of the channel length. For several references,[9,41,59–61] some parameters were estimated from electrical characteristics. The boxes show the 25th and 75th percentiles whereas the whiskers represents the 5th and 95th percentiles. The empty square in the boxes shows the mean value.

Table 1 Merits and demerits of the nanonet device comparing with single nanowire FET in the same configuration.

	Nanonet FET	**Single NWFET**
Integration process	*Standard optical lithography*	*Need for lithography alignments regarding the SiNW locations*
Channel length / width	*From microns to millimeters / From tens to hundreds microns*	*Shorter than SiNW length / SiNW diameter*
Process reliability	*100% of devices are functional*	*Numerous defective devices due to misalignments*
Process throughput	*High*	*Low*
Device reproducibility	*High*	*Low*
Transistor performances	I_{on}/I_{off}~10^5 *SS~1V.dec*$^{-1}$	I_{on}/I_{off}~10^5 *SS~0.7V.dec*$^{-1}$

4 Conclusions

In this paper, we have demonstrated the fabrication of highly performant and reproducible SiNW-based field effect transistors by a highly reliable technological process involving solely standard optical lithography techniques. Using a large number of SiNW self-assembled in networks called nanonets, we developed a low temperature (≤400°C) and cost-effective process which is suitable for mass production over large areas. Compared to single SiNW-based device, the collective use of SiNWs allows to facilitate the SiNW integration, guarantee the device functionality and improve the device-to-device reproducibility.

For the first time, the averaging effect associated to the network geometry has been statistically demonstrated: as more nanowires are involved in each conduction path, by an averaging effect, the important morphological differences between nanowires no longer affect the electronic properties.

Finally, electrical properties were significantly enhanced via the alumina encapsulation. On the basis of statistical characterizations, it is now obvious that silicon nanonet FETs exhibit outstanding electrical performances which can compete with single SiNW-based transistor whose performances are reported in the literature. Compared to NW devices whose current integration techniques are complex, we are deeply convinced that our new generation of SiNW-based transistors may present interesting features in the context of the “More Than Moore” roadmap. This technological building block opens up new opportunities, ranging from ultra-sensitive biological sensors to flexible electronic devices.

Electronic Supplementary Material

The online version of this article contains supplementary material about the length and diameter of nanowires used in the study and output characteristics of 8-nm alumina encapsulated silicon nanonet field effect transistors, which is available to authorized users.

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References

[1] N.P. Dasgupta, J. Sun, C. Liu, S. Brittman, S.C. Andrews, J. Lim, H. Gao, R. Yan, P. Yang, Adv. Mater. 26 (2014) 2137–2184.

[2] A.M. Ionescu, (2008) 4–6.

[3] W. Arden, M. Brillouët, P. Cogez, M. Graef, B. Huizing, R. Mahnkopf, ITRS: More-than-Moore, 2010.

[4] G.E. Moore, Proc. IEEE 86 (1998) 82–85.

[5] Y. Li, F. Qian, J. Xiang, C.M. Lieber, Mater. Today 9 (2006) 18–27.

[6] Y. Cui, X. Duan, J. Hu, C.M. Lieber, J. Phys. Chem. B 104 (2000) 5213–5216.

[7] V. Schmidt, J. V. Wittemann, S. Senz, U. Gösele, Adv. Mater. 21 (2009) 2681–2702.

[8] M.J. Crane, P.J. Pauzauskie, J. Mater. Sci. Technol. 31 (2015) 523–532.

[9] Y. Cui, Z. Zhong, D. Wang, W.U. Wang, C.M. Lieber, Nano Lett. 3 (2003) 149–152.

[10] J. Appenzeller, J. Knoch, E. Tutuc, M. Reuter, S. Guha, in: 2006 Int. Electron Devices Meet., IEEE, 2006, pp. 1–4.

[11] O. Hayden, M.T. Björk, H. Schmid, H. Riel, U. Drechsler, S.F. Karg, E. Lörtscher, W. Riess, Small 3 (2007) 230–234.

[12] Y.L. Bunimovich, Y.S. Shin, W.S. Yeo, M. Amori, G. Kwong, J.R. Heath, J. Am. Chem. Soc. 128 (2006) 16323–16331.

[13] Z. Li, B. Rajendran, T.I. Kamins, X. Li, Y. Chen, R.S. Williams, Appl. Phys. A 80 (2005) 1257–1263.

[14] G. Jayakumar, A. Asadollahi, P.E. Hellström, K. Garidis, M. Östling, Solid. State.

Electron. 98 (2014) 26–31.
[15] G. Rosaz, B. Salem, N. Pauc, A. Potié, P. Gentile, T. Baron, Appl. Phys. Lett. 99 (2011) 193107.
[16] Y. Cui, C.M. Lieber, Science (80-.). 291 (2001) 851–853.
[17] Y. Huang, X. Duan, Y. Cui, L.J. Lauhon, K.H. Kim, C.M. Lieber, Science (80-.). 294 (2001) 1313–1317.
[18] Y. Cui, Q. Wei, H. Park, C.M. Lieber, Science (80-.). 293 (2001) 1289–1292.
[19] J. Hahm, C.M. Lieber, Nano Lett. 4 (2004) 51–54.
[20] M.Y. Shen, B.R. Li, Y.K. Li, Biosens. Bioelectron. 60 (2014) 101–111.
[21] M.O. Noor, U.J. Krull, Anal. Chim. Acta 825 (2014) 1–25.
[22] R. Ahmad, T. Mahmoudi, M.S. Ahn, Y.B. Hahn, Biosens. Bioelectron. 100 (2018) 312–325.
[23] M. Liu, Z. Wu, W.M. Lau, J. Yang, Nano-Micro Lett. 4 (2012) 142–153.
[24] G. Grüner, J. Mater. Chem. 16 (2006) 3533–3539.
[25] J.Y. Lee, S.T. Connor, Y. Cui, P. Peumans, Nano Lett. 8 (2008) 689–692.
[26] M.A. Meitl, Y. Zhou, A. Gaur, S. Jeon, M.L. Usrey, M.S. Strano, J.A. Rogers, Nano Lett. 4 (2004) 1643–1647.
[27] R.C. Tenent, T.M. Barnes, J.D. Bergeson, A.J. Ferguson, B. To, L.M. Gedvilas, M.J. Heben, J.L. Blackburn, Adv. Mater. 21 (2009) 3210–3216.
[28] S. Acharya, A.B. Panda, N. Belman, S. Efrima, Y. Golan, Adv. Mater. 18 (2006) 210–213.
[29] Z. Wu, Z. Chen, X. Du, J.M. Logan, J. Sippel, M. Nikolou, K. Kamaras, J.R. Reynolds, D.B. Tanner, A.F. Hebard, A.G. Rinzler, Science 305 (2004) 1273–1276.
[30] W. Xu, Q. Xu, Q. Huang, R. Tan, W. Shen, W. Song, J. Mater. Sci. Technol. 32 (2016) 158–161.
[31] M. Legallais, T.T.T. Nguyen, M. Mouis, B. Salem, E. Robin, P. Chenevier, C. Ternon, Solid. State. Electron. 143 (2018) 97–102.
[32] F. Morisot, C. Zuliani, J. Luque, Z. Ali, M. Mouis, V.H. Nguyen, D. Muñoz-Rojas, O. Lourhzal, M. Texier, T.W. Cornelius, C. Ternon, Mater. Res. Express 6 (2019) 084004.
[33] P. Serre, M. Mongillo, P. Periwal, T. Baron, C. Ternon, Nanotechnology 26 (2015) 1–10.
[34] K. Heo, E. Cho, J.E. Yang, M.H. Kim, M. Lee, B.Y. Lee, S.G. Kwon, M.S. Lee, M.H. Jo, H.J. Choi, T. Hyeon, S. Hong, Nano Lett. 8 (2008) 4523–4527.
[35] D. Whang, S. Jin, Y. Wu, C.M. Lieber, Nano Lett. 3 (2003) 1255–1259.
[36] E. Mulazimoglu, S. Coskun, M. Gunoven, B. Butun, E. Ozbay, R. Turan, H.E. Unalan, Appl. Phys. Lett. 103 (2013) 1–5.
[37] C. Ternon, P. Serre, J.M. Lebrun, V. Brouzet, M. Legallais, S. David, T. Luciani, C. Pascal, T. Baron, J.M. Missiaen, Adv. Electron. Mater. 1 (2015) 1–8.
[38] R.S. Wagner, W.C. Ellis, Appl. Phys. Lett. 4 (1964) 89.
[39] S. Liang, G. He, D. Wang, F. Qiao, J. Mater. Sci. Technol. 35 (2019) 769–776.
[40] Y. Liu, L. Zhu, L. Guo, H. Zhang, H. Xiao, J. Mater. Sci. Technol. 30 (2014) 835–838.
[41] G. Rosaz, B. Salem, N. Pauc, P. Gentile, A. Potié, A. Solanki, T. Baron, Semicond. Sci. Technol. 26 (2011) 085020.

[42] B. Reddy, B.R. Dorvel, J. Go, P.R. Nair, O.H. Elibol, G.M. Credo, J.S. Daniels, E.K.C. Chow, X. Su, M. Varma, M.A. Alam, R. Bashir, Biomed. Microdevices 13 (2011) 335–344.

[43] W. Zhou, X. Dai, T.M. Fu, C. Xie, J. Liu, C.M. Lieber, Nano Lett. 14 (2014) 1614–1619.

[44] F. Morisot, V.H. Nguyen, C. Montemont, T. Maindron, D. Muñoz-Rojas, M. Mouis, M. Langlet, C. Ternon, Nanotechnology (2019). Doi 10.1088/1361-6528/ab2aa5

[45] K.R. Williams, K. Gupta, M. Wasilik, J. Microelectromechanical Syst. 12 (2003) 761–778.

[46] N. Elfström, R. Juhasz, I. Sychugov, T. Engfeldt, A.E. Karlström, J. Linnros, Nano Lett. 7 (2007) 2608–2612.

[47] X.P.A. Gao, G. Zheng, C.M. Lieber, Nano Lett. 10 (2010) 547–552.

[48] J. Li, Y. Zhang, S. To, L. You, Y. Sun, ACS Nano 5 (2011) 6661–6668.

[49] Q. Cao, M.G. Xia, M. Shim, J.A. Rogers, Adv. Funct. Mater. 16 (2006) 2355–2362.

[50] S. Kumar, N. Pimparkar, J.Y. Murthy, M.A. Alam, Appl. Phys. Lett. 88 (2006) 123505.

[51] M.K. Joo, M. Mouis, D.Y. Jeon, G.T. Kim, U.J. Kim, G. Ghibaudo, J. Appl. Phys. 114 (2013) 154503.

[52] L. Hu, D.S. Hecht, G. Grüner, Chem. Rev. 110 (2010) 5790–5844.

[53] E.S. Snow, P.M. Campbell, M.G. Ancona, J.P. Novak, Appl. Phys. Lett. 86 (2005) 033105.

[54] S.M. Sze, K.K. Ng, Physics of Semiconductor Devices, Third Edition, Wiley-Interscience, 2006.

[55] T. Cazimajou, M. Legallais, M. Mouis, C. Ternon, B. Salem, G. Ghibaudo, Solid. State. Electron. 143 (2018) 83–89.

[56] C. Kocabas, N. Pimparkar, O. Yesilyurt, S.J. Kang, M.A. Alam, J.A. Rogers, Nano Lett. 7 (2007) 1195–1202.

[57] S. Kumar, J.Y. Murthy, M.A. Alam, Phys. Rev. Lett. 95 (2005) 1–4.

[58] T.T.T. Nguyen, T. Cazimajou, M. Legallais, T. Arjmand, V.H. Nguyen, M. Mouis, B. Salem, E. Robin, C. Ternon, Nano Futures. 3 (2019) 025002.

[59] K. Byon, D. Tham, J.E. Fischer, A.T. Johnson, Appl. Phys. Lett. 90 (2007) 143513.

[60] W.M. Weber, L. Geelhaar, A.P. Graham, E. Unger, G.S. Duesberg, M. Liebau, W. Pamler, C. Chèze, H. Riechert, P. Lugli, F. Kreupl, Nano Lett. 6 (2006) 2660–2666.

[61] G. Zheng, W. Lu, S. Jin, C.M. Lieber, Adv. Mater. 16 (2004) 1890–1893.

Figure caption list

Fig. 1 Schematic representation of the seven main fabrication steps of the silicon nanonet bottom-gate field effect transistors: (i) SiNW growth, (ii) fabrication and transfer of nanonets onto the substrate, (iii) SiNW-SiNW junction sintering, (iv) alumina encapsulation, (v) contact fabrication, (vi) lift-off and (vii) silicidation

Fig. 2 Si nanonet-based field effect transistor (Si-NN FET) with a bottom gate configuration. (A) Scheme of Si-NN FET. One example of conducting path is highlighted in red for illustration. (B) SEM top-view of Si-NN FET with a channel length (L_c) of 20 µm.

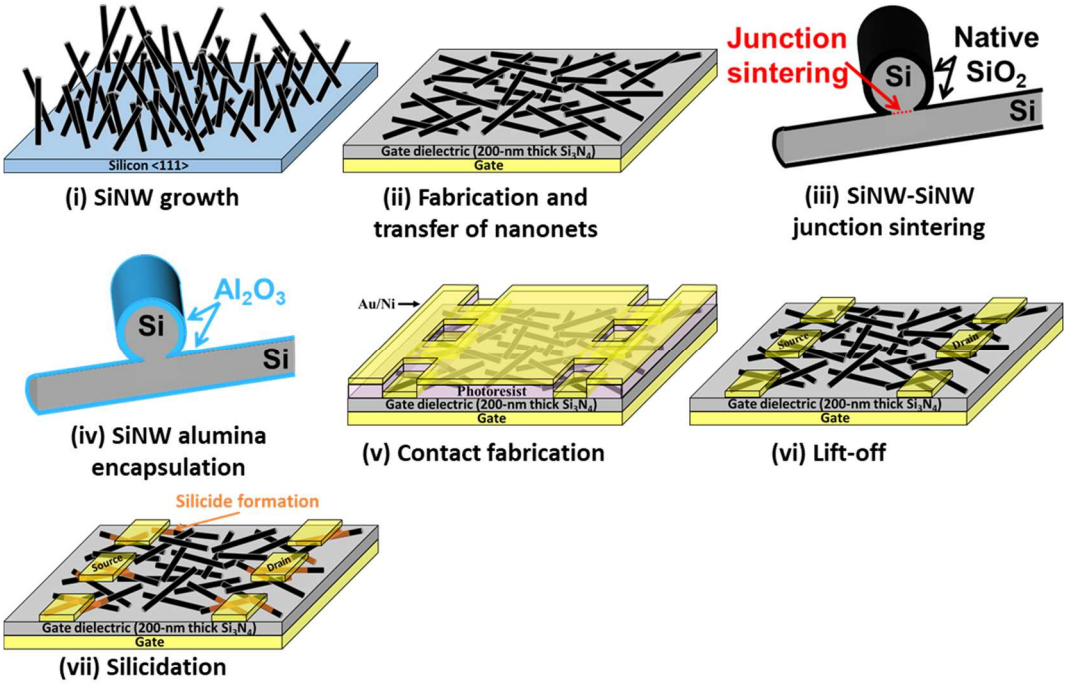
Fig. 3 Comparison between sintered Si-NN coated by (A, C) natively grown silicon dioxide and encapsulated by (B, D) alumina deposited using ALD. (A, B) refers to top-view SEM images of nanonets while (C, D) are cross-sectional schemes of 3 coated SiNWs: 1 sectioned in the length and 2 according to the diameter. For (C), the mean and standard deviation of SiNW length (L_{SiNWs}) and diameter (D_{SiNWs}) are indicated. For (D), due to conformal coating with ALD, alumina is deposited simultaneously on SiNWs and onto the substrate whereas SiNW-SiNW junctions and underneath SiNW portions are considered alumina-free.

Fig. 4 Transfer characteristic comparison between devices constituted by either native 2 nm-SiO_2 Si-NN or 8-nm alumina coated Si-NN. For both, the channel length (L_c) is 20 µm and the drain voltage (V_d) was set at -4V.

Fig. 5 Effect of the alumina thickness on the On current (I_{On}), extracted at -25V, and the subthreshold slope (SS). 0 nm of alumina corresponds to 2-nm thick layer of native SiO_2. For all transistors, the channel length (L_c) is 20 µm and the drain voltage (V_d) was set at -4V. The boxes show the 25th and 75th percentiles whereas the whiskers represents the 5th and 95th percentiles. The empty square in the boxes shows the mean value.

Fig. 6 Reproducibility of the On and Off current for transistors based on native SiO_2 Si-NNs (full symbol) and 8-nm alumina encapsulated Si-NNs (empty symbol) for 20 µm (square) and 30 µm (triangle) long channel. For native SiO_2 Si-NN based devices, no current is observed when channel length is 30 µm. The On-to-Off ratio (I_{On}/I_{Off}) is indicated by the dashed line. I_{On} and I_{Off} were extracted à -25V and +25V, respectively.

Fig. 7 Comparison of electrical performances between 8-nm alumina encapsulated Si NN-FETs (from this work) and single SiNW-FETs with a bottom-up approach and a bottom-gate configuration as reported in the literature[9,11,41,59–61]. (A) On-to-Off ratio (I_{On}/I_{Off}) and (B) subthreshold slope (SS) as a function of the channel length. For several references,[9,41,59–61] some parameters were estimated from electrical characteristics. The boxes show the 25th and 75th percentiles whereas the whiskers represents the 5th and 95th percentiles. The empty square in the boxes shows the mean value.



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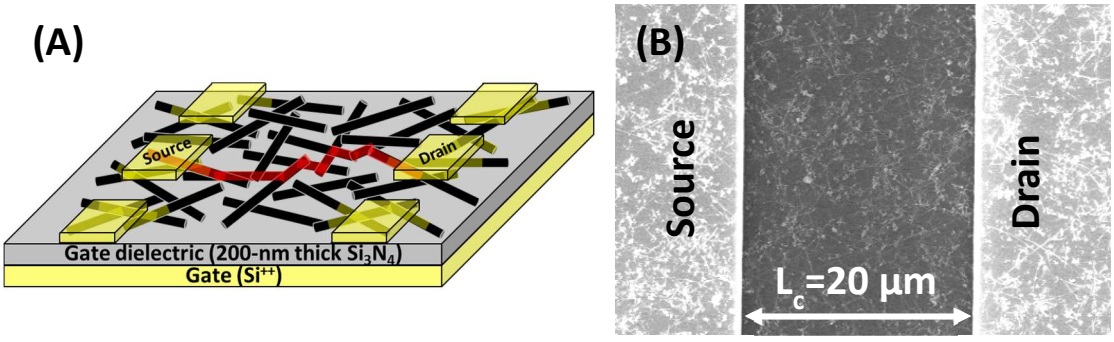

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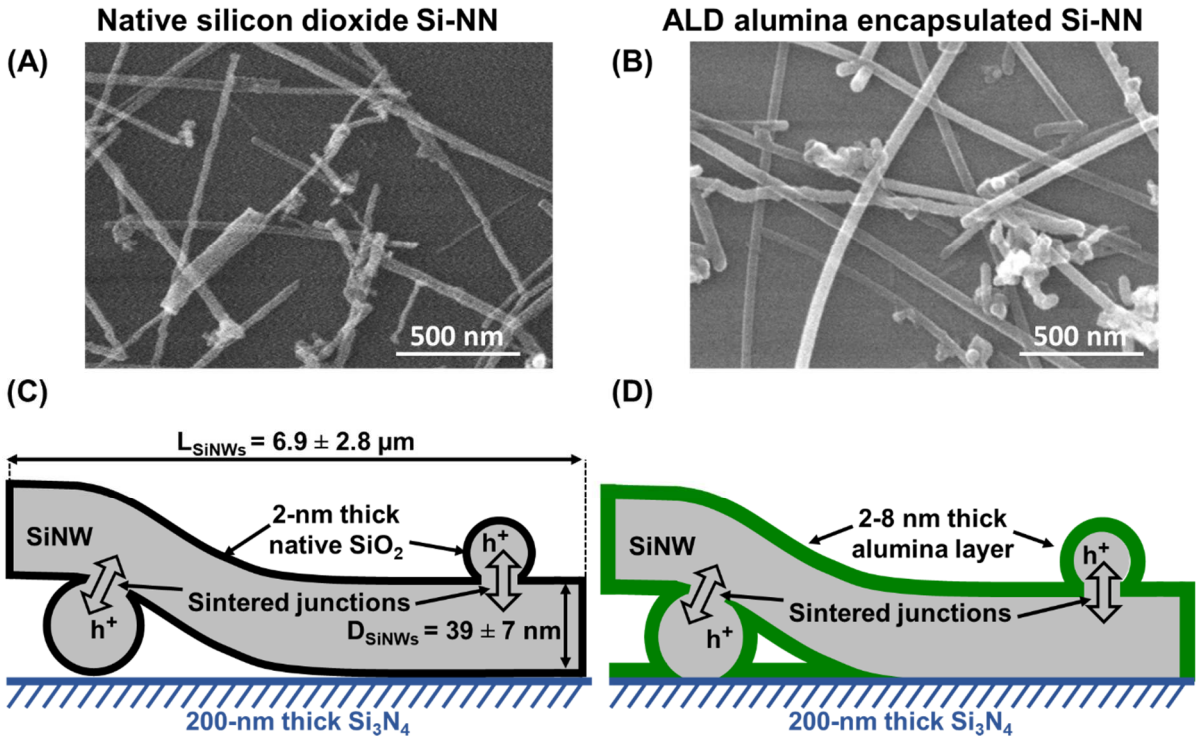

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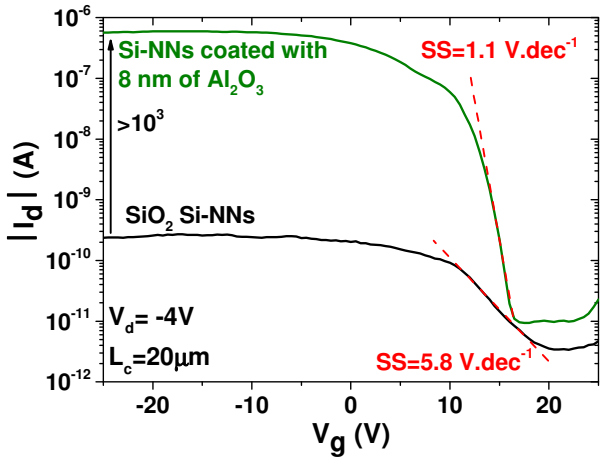

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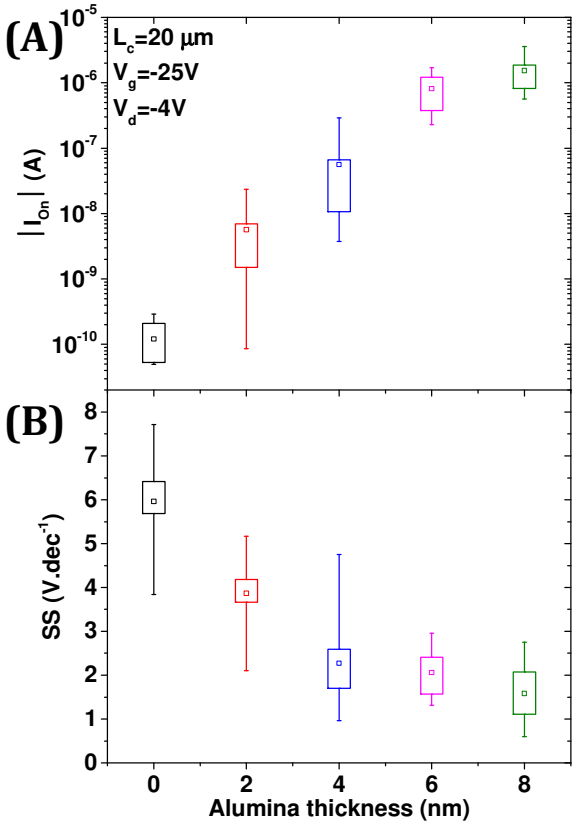

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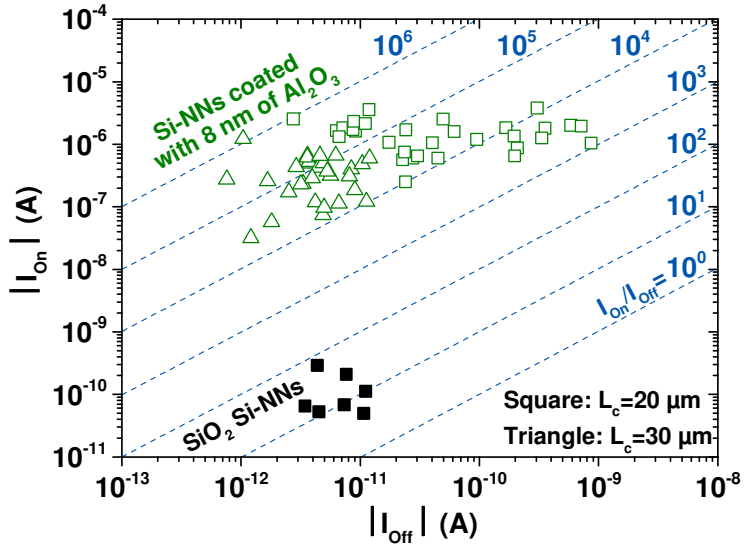

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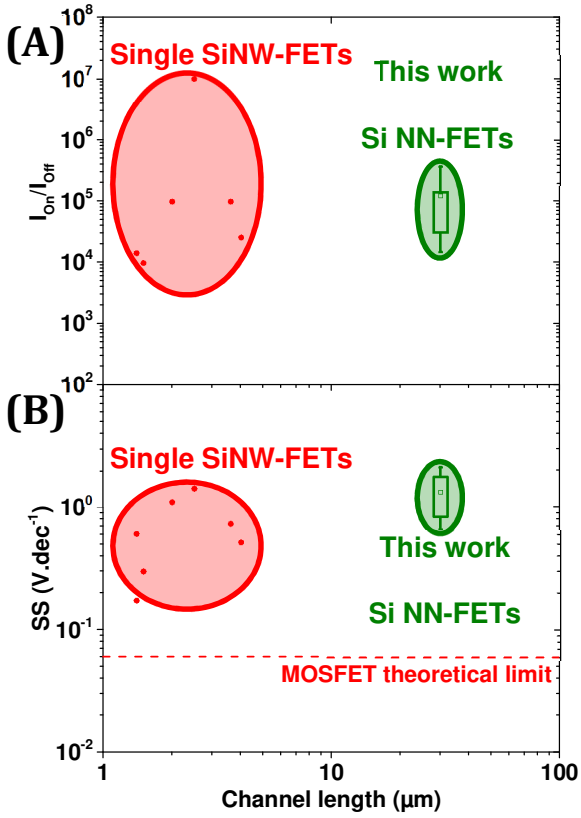

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Supplementary Material

Material Engineering of Percolating Silicon Nanowire Networks for Reliable and Efficient Electronic Devices

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S1 Length and diameter statistics of silicon nanowires.

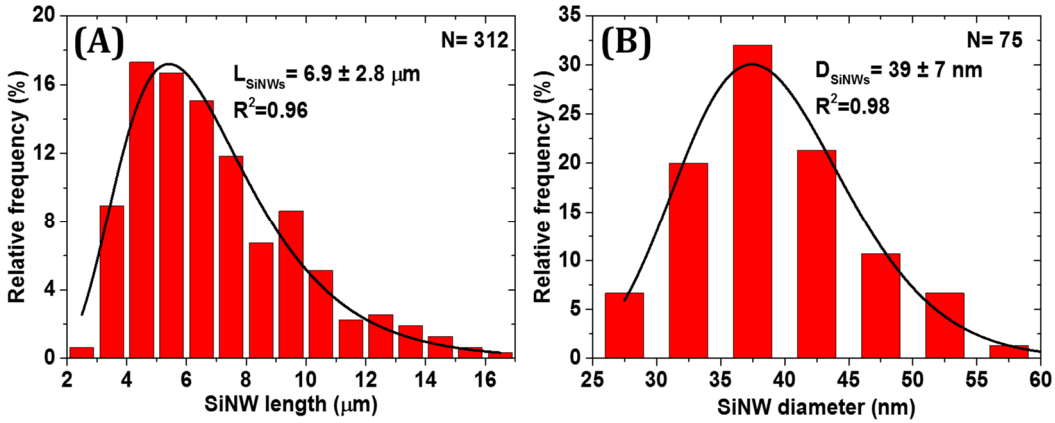

Fig. S1 Statistics relative to (A) the length (L_{SiNWs}) and (B) the diameter (D_{SiNWs}) of silicon nanowires (SiNWs) used to fabricate networks. Both parameters were fitted with a log-normal function. 'N' indicates the number of measured nanowires.

S2 Output characteristics of 8-nm alumina encapsulated silicon nanonet field effect transistors for different channel lengths.

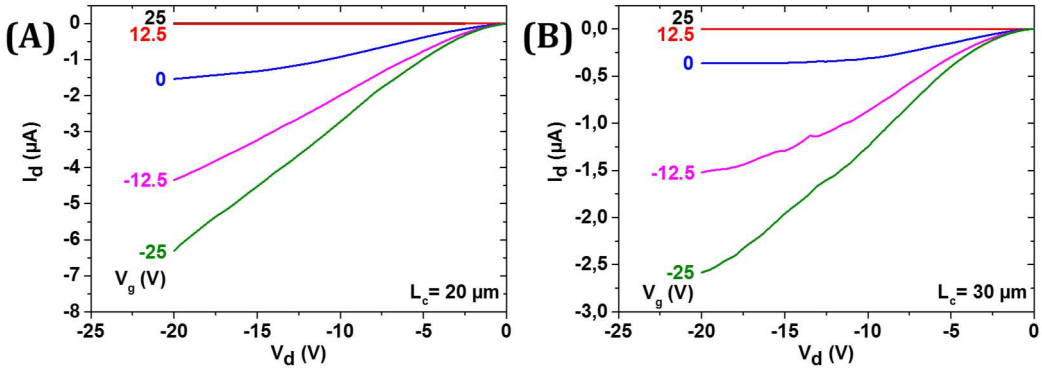

Fig. S2 Output characteristics (I_d-V_d) of 8-nm alumina encapsulated silicon nanonet field effect transistors with a channel length (L_c) of (A) 20 µm and (B) 30 µm. Gates voltages (V_g) are marked on the curves.

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Graphical abstract