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# Engineering self-assembly of a high- $\chi$ block copolymer for large area fabrication of transistors based on functional graphene nanoribbon arrays

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## Abstract

Graphene presents a real need for patterning into very narrow nanostructures to open up a bandgap and tune its electrical properties by quantum confinement. A self-assembled silicon-based block copolymer (BCP) is used to pattern CVD-grown graphene to fabricate graphene nanoribbon (GNR) arrays. Best BCP lithographic performances are obtained when the BCP is spin-coated and annealed directly on graphene. Self-assembly on large surfaces (1 cm<sup>2</sup>) is achieved in a few minutes and 11-nm-width GNR

are finally obtained. Electrical characterization of these structures such as bandgap opening is carried out to confirm the electronic behavior of the graphene nanoribbons. Bandgap values of the order of 70 meV were measured. The BCP self-assembly process proposed is scalable and low cost, and is well-suited for integration with existing semiconductor fabrication techniques. The lithography procedure developed in this investigation could be generalized to fabricate graphene nanomeshes or quantum dots on large surfaces. Also, other 2D materials and heterostructures could be concerned, for to the study of innovative nano-structured materials and functional devices.

## Keywords

CVD graphene, PS-*b*-PDMS, self-assembly, nanolithography, nanoribbons, field-effect transistor

## Introduction

Block copolymer (BCP) lithography builds up nowadays as a surrogate patterning technique capable of producing efficiently sub-10 nm features. Among its counterparts, e.g. electron-beam, ion-beam, deep UV and multiple patterning lithographies,<sup>1-3</sup> BCP lithography has a large advantage in terms of cost of implementation, scalability and throughput. These three factors are essential to fulfill and exploit the current demand in applications needing ultra high-resolution patterning.

BCP lithography is based on a thermodynamics-governed self-assembly mechanism. In equilibrium conditions, BCPs macromolecules self-assemble into ordered periodical structures,<sup>4</sup> which can be used as lithography masks for device fabrication. The opportunity to create sub-10 nm periodical lengths is closely linked to a larger chemical incompatibility between the polymer blocks. This contrast is usually designated as the Flory-Huggins interaction parameter  $\chi$  by the BCP theory.<sup>5</sup>

Lately, research on BCP synthesis has been focused on high- $\chi$  systems, to name a few: poly(styrene)-*block*-poly(4-vinylpyridine) (PS-*b*-P4VP), poly(styrene)-*block*-poly(dimethylsiloxane) (PS-*b*-PDMS) and poly(1,1-dimethylsilacyclobutane)-*block*-poly(styrene) (PDMSB-*b*-PS).<sup>6-8</sup> They all aim to replace a first generation of BCP systems such as poly(styrene)-*block*-poly(methyl methacrylate) (PS-*b*-PMMA) and poly(styrene)-*block*-poly(ethylene oxide) (PS-*b*-PEO) with rather low- $\chi$  values ( $\chi < 0.1$  at 298 K) limiting the attainable resolution to around 15 nm.<sup>9</sup>

Apart from resolution, a high etching selectivity make PS-*b*-PDMS thin films technologically attractive as performant templates for nanolithography. A high assembly kinetics is attainable through thermal annealing for PS-*b*-PDMS having low molecular weight. Nevertheless, the use of PS-*b*-PDMS faces issues concerning the domain orientation control due to a high surface energy contrast between the blocks ( $\gamma_{PS} = 40.7 \text{ mJ/m}^2$  vs.  $\gamma_{PDMS} = 19.8 \text{ mJ/m}^2$ ).<sup>10,11</sup> Consequent difficulties in obtaining the desired equilibrium morphology and stacking of the BCP thin film were solved by a functionalization of the substrates with hydroxy-terminated polymers.

Within the context of emerging 2D materials, among them graphene and transition metal dichalcogenides,<sup>12,13</sup> PS-*b*-PDMS nanolithography encounters further challenges. 2D materials need high-resolution patterning as an effective method to enhance a specific property.<sup>14,15</sup> Such is the case of the electronic bandgap in graphene through an accurate structuration.<sup>16</sup> PS-*b*-PDMS self-assembly on atomic-thick substrates establishes proper constraints in the morphology control since the usual functionalizations could irreversibly damage their structural and electrical properties. For this reason, dealing with graphene requires special consideration regarding its physico-chemical state during the self-assembly process as well as a critical dimensional characterization on an atomic scale during patterning.

The few studies that have been conducted on the self-assembly of cylindrical PS-*b*-PDMS on CVD-grown graphene to produce graphene nanoribbons (GNR)<sup>17-19</sup> usually use the unconventional solvent vapor annealing to trigger self-assembly. Device-oriented studies favor

thermal annealing as an effort to exploit the PS-*b*-PDMS on manufacture-adapted procedures.<sup>20,21</sup> In this context, additional investigations are required on the self-assembly mechanism on graphene. It includes the searching of the equilibrium conditions at which the cylinder morphology can be obtained on large surfaces to guarantee the ensuing development of GNR-based devices.

This study aims at investigating the cylindrical PS-*b*-PDMS self-assembly on CVD-grown graphene by thermal means to produce GNRs arrays over large areas. Across the study of the BCP/graphene interface and their interactions, we highlight how the chemical state of the CVD-grown graphene impacts on the sensitive self-assembly process. Dealing with a graphene surface energy modification through a thermal pre-annealing, we achieve a morphology control of the PS-*b*-PDMS thin film adapted for nanolithography without altering the graphene properties. Furthermore, the large-area patterning of graphene is shown with an exhaustive characterization. Finally, the development of back-gate field-effect transistors (FET) based on GNRs arrays allowed to verify the effect of the graphene structuration on its conductive properties with the transition from metallic to semiconductor behavior.

## Experimental section

### Graphene and block copolymer

Monolayer CVD-grown graphene on 300-nm SiO<sub>2</sub> on P++ < 100 > Si 4-in wafer, was obtained from Graphenea (Spain); usually transferred by a wet transfer process. The graphene/SiO<sub>2</sub> wafer was carefully cleaved into 1 cm<sup>2</sup> samples. Cylinder-forming PS-*b*-PDMS BCP (M<sub>w</sub>=11.5 kg/mol, PDI=1.08, f<sub>PDMS</sub>=33%) were purchased from Polymer Source Inc. (Canada) and microelectronic-grade propylene glycol methyl ether acetate (PGMEA) was used as the solution solvent. A BCP monolayer was deposited directly on the CVD-grown graphene. For this, a BCP solution of 1 wt% was spin-coated at different spin speeds. The final BCP thickness and the spin speed were correlated by ellipsometry measurements and

estimated at  $18 \pm 2$  nm for 1800 rpm. A vacuum drying oven at  $10^{-3}$  mbar was used for graphene surface energy modification as well as a hot plate for annealing treatment at different temperatures and time to achieve the cylinder-forming self-assembly of the BCP. After thermal annealing, samples were first etched by  $\text{CF}_4$  plasma (6 s, 4 mTorr, 500 W) to remove the top-segregated PDMS layer; then a  $\text{HBr}/\text{O}_2$  plasma (14 s, 5 mTorr, 150 W) etched both the PS block and the unexposed graphene. BCP mask stripping was performed with HF and GNRs cleaning with  $\text{H}_2$  plasmas (20 s, 200 mTorr, 800 W).

Fig. 1 resumes the entire procedure developed in this study in order to perform the self-assembly of a PS-*b*-PDMS BCP to obtain a lithography mask for graphene patterning. This method allows an effective large-area integration of FETs based on dense 11-nm-width GNR arrays. Our strategy includes: (1) the use of CVD-grown graphene on 4-inch wafers deposited on 300nm- $\text{SiO}_2$ , which is suitable for large-scale device fabrication; (2) eventually the annealing of CVD graphene on  $\text{SiO}_2$  under vacuum ( $10^{-3}$  mbarr) for surface energy modification at 170 °C for 1 h and finally (3) the direct spin-coating of the PS-*b*-PDMS solution and its thermal annealing for 3 min, enabling spontaneous phase separation and formation of densely packed periodic arrays of cylindrical BCP nanodomains.

## Characterizations

*Observations.* Scanning electron microscopy (SEM) images were performed at 30 kV with a field emission electron source (Hitachi S-5000). Sample preparations for transmission electron microscopy (TEM) were carried out in a Helios 450S-FEI dual beam microscope. A small sample was extracted and thinned to approximately 100-nm-width, after the deposition of 1- $\mu\text{m}$ -Pt on the BCP thin film. An *in-situ* observation was finally carried out using in scanning mode (STEM) in the same equipment or a JEM-2100F instrument was used for TEM observations at an electron acceleration voltage of 200 KV.

*Contact angle.* Static contact angles were measured by the drop shape analyzer DSA100 from Krüss (Germany). All measurements were performed at room temperature (25 °C) by

depositing a water droplet with 7  $\mu\text{L}$  volume on the surface. The contact angle was measured based on the image captured by a CDD camera using the ADVANCE software.

*X-ray photoelectron spectroscopy.* The chemical state of CVD-grown graphene was studied by XPS with a customized Thermo Electron Theta 300 spectrometer. Measurements were achieved at a pressure of  $10^{-9}$  mbar using a monochromatic X-ray source Al-K $\alpha$  (1486.6 eV). An electron flood gun was turned on during acquisitions to reduce surface charging. The overall energy resolution of the analysis was 0.5 eV. CASAXPS software was used for fitting the C1s peak.

*Raman spectroscopy.* Raman mapping of GNRs arrays was performed using the LabRAM HR Evolution equipment from Horiba Scientific. Measurements were performed using a 70x objective with a green laser having an excitation wavelength of 532 nm. The laser power was 4 mW and the acquisition time was of the order of 30 seconds. Lateral focus of the laser was  $\sim 1\mu\text{m}$ . Mapping area was  $100\ \mu\text{m}^2$ , scanning from 0 to 10  $\mu\text{m}$  in both  $x$  and  $y$  directions with a step of 2.5  $\mu\text{m}$ .

*Atomic force microscopy.* The GNRs arrays were characterized dimensionally by an AFM Bruker Dimension FastScan, using the automatic mode with a Si tip. Typical parameters for image acquisition used here were 512 lines with a scan rate of 1.98 Hz. Scan size of images was  $1\ \mu\text{m}^2$ — and the image treatment was performed using the software Gwyddion (<http://gwyddion.net/>).

## **Electrical measurements**

The photolithography transferred pattern method (PTP method) was used to directly deposit metallic contacts on GNRs as follows: a Si < 100 > P++ sacrificial substrate was cleaved in  $1\ \text{cm}^2$  from 4-in wafers. Then a positive photoresist AZ 1512HS from Microchemicals GmbH, Germany, was spin-coated on Si samples. After UV exposition, photoresist was developed in AZ 1:4 developer solution to remove the exposed zones. Deposition of 100 nm of Au was achieved with a PLASSYS, France, equipment in clean room conditions. Au

on resist was lifted-off for 1 h with acetone and a final rinsing with iso-propanol. A second stage consisted in spin-coating PMMA A9 from Microchemicals directly on Au contacts. The PMMA/gold layer was then detached from the substrate with a substrate etching in NaOH 1M solution at 50 °C until complete detachment. The PMMA/gold film was then transferred and placed on the GNRs sample surface and the stack was dried in the air. Several cycles of 30 s in acetone, 10 s in iso-propanol and N<sub>2</sub> flow drying were repeated until PMMA removal. Finally a soft-bake at 100 °C for 1 h in vacuum (10<sup>-3</sup> mbar) to build contact bonding with GNRs was required.

The contacted sample was finally composed of a P++ (100) Si substrate, a 300-nm silica film, patterned graphene and 2 on-top Au contacts separated of 2 μm. This stack constitutes the back-gated FET used to prove the bandgap opening in GNR arrays. Electrical measurements were performed with a Keithley 4200-SCS equipment. Samples were characterized with the I<sub>DS</sub> vs. V<sub>DS</sub> curve from +0.5 V to -0.5 V at a fixed V<sub>G</sub> = 0 V, and then with the transcharacteristics curve I<sub>DS</sub> vs. V<sub>G</sub> from +30 V to -30 V at a constant V<sub>DS</sub> = 0.2 V. V<sub>DS</sub> and I<sub>DS</sub> are defined as the voltage and current between transistor drain and source, respectively.

## Results and discussion

### Self-assembly of PS-*b*-PDMS

The typical morphology obtained when using the PS-*b*-PDMS BCP (M<sub>n</sub> =16kg/mol, f<sub>PDMS</sub> = 33%) is PDMS cylindrical microdomains in a PS matrix. We chose to work with this asymmetric polymer because it allows the formation of objects  $\lesssim$  10 nm with a natural period of 20 nm ( $L_0$ ),<sup>22</sup> which is interesting for graphene patterning.

The self-assembly behavior of the PS-*b*-PDMS was studied directly on CVD-grown graphene samples. A direct spin-coating of the BCP on graphene was used to avoid underlayers such as resists, brush polymers or even insulator materials.<sup>23</sup> Also, we found that direct spin-



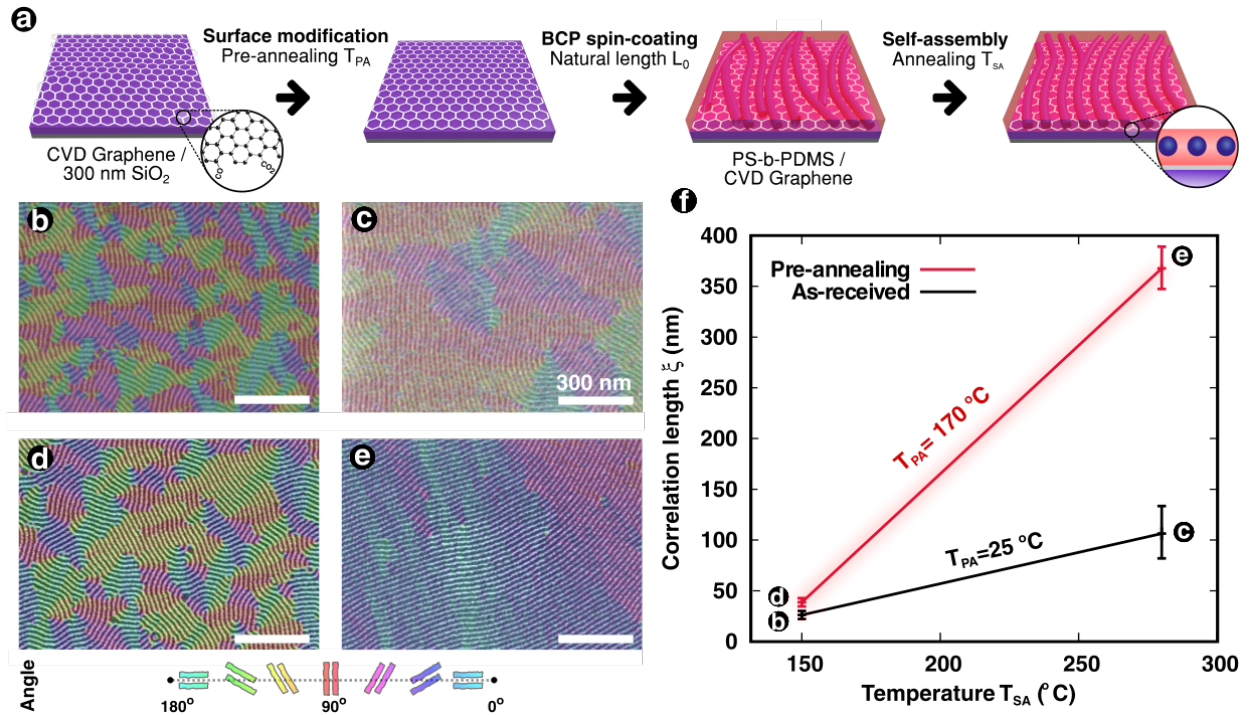


Figure 1: (a) Graphic representation of the CVD-grown graphene patterning on large surfaces through thermal modification of the surface energy, direct spin-coating of the high- $\chi$  BCP PS-*b*-PDMS and its cylindrical self-assembly by thermal means. (b-e) Top-view SEM images of the self-assembled PS-*b*-PDMS and their corresponding orientation maps. (f) Correlation lengths ( $\xi$ ) from the orientation maps measured at different self-assembly annealing temperatures ( $T_{SA}$ ), eventually with a thermal pre-annealing treatment at  $T_{PA} = 170$  °C.

coating was more efficient than using transfer layers, in particular at the resist stripping step. Indeed, this step is critical as GNRs could be damaged or contaminated, impacting their electronic properties.

Hereinafter, two different annealing temperatures need to be defined. First, the temperature of pre-annealing ( $T_{PA}$ ) for graphene surface energy modification, performed in vacuum to avoid graphene oxidation. Then, the temperature of self-assembly ( $T_{SA}$ ) used in air to trigger BCP organization. Latest advances on the self-assembly of the high- $\chi$  BCPs show an improvement in the microphase ordering of the PS-*b*-PDMS with a defect reduction by shortening time and increasing annealing temperature ( $300\text{ }^\circ\text{C} < T_{SA} < 700\text{ }^\circ\text{C}$ ).<sup>24,25</sup> We studied the effect of higher temperatures on the final microphase ordering by annealing up to  $T_{SA}=280\text{ }^\circ\text{C}$ . We used this upper temperature to avoid any degradation of the graphene properties, as thermal stability in graphene has been observed up to  $300\text{ }^\circ\text{C}$  ~~both~~ in standard cleanroom atmosphere.<sup>26,27</sup>

For a better legibility of pattern ordering and grain sizes, orientation mappings are displayed in each SEM image of Figs. 1b-e. Moreover, the measurement of the correlation lengths ( $\xi$ ) are depicted in Fig. 1f, as this parameter allows to quantify the microphase ordering.

When using  $T_{SA}=280\text{ }^\circ\text{C}$ , a cylinder-morphology is achieved (Fig. 1c) as expected, with  $\xi$  measured at 106 nm. This result shows a light improvement in the microphase ordering, in comparison with a lower temperature to generate self-assembly. Fig. 1b shows the top-view SEM image at  $T_{SA}=150\text{ }^\circ\text{C}$ , corresponding to  $\xi = 26\text{ nm}$ . Despite an improvement in the microphase ordering by increasing the annealing temperature, both correlation lengths are just a few times the natural length  $L_0$  which is considered a poor self-assembly ( $\xi \lesssim 100\text{ nm}$ ).

In thin film, the self-assembly process is dominated by a significant interface free energy contribution ( $F_{\text{interface}}$ ) to the total free energy  $F$  of the BCP thin film.<sup>28</sup> In our case, interface interactions between BCP and graphene has a strong influence on the phase separation

and the orientation of the blocks. Modification and control of the graphene surface energy should allow a precise control of the wetting, BCP orientation and long-range order. Indeed, Kim and coworkers reported a morphology control of BCP thin films by reducing thermally graphene oxide films.<sup>29</sup>

Similar to graphene oxide reduction, we achieved a thermal pre-annealing of CVD-graphene substrates to deal with surface energy modification. As a reminder, PMMA is commonly used as a graphene transfer carrier polymer from <sup>the</sup> Cu growth substrate to the target substrate (SiO<sub>2</sub> in this case).<sup>30</sup> A PMMA coating forms covalent bonds with graphene,<sup>31</sup> which changes significantly the graphene surface state from what it is theoretically predicted.<sup>32</sup> Moreover, molecular absorption of H<sub>2</sub>O and O<sub>2</sub> molecules and carbon contaminants from air during graphene processing could impact its properties<sup>33</sup>. Actually, received graphene surfaces behave rather as a PMMA surface, as evidenced by contact angle measurements (Fig. S1); the graphene surface is rather hydrophilic.

Indeed, by a thermal annealing treatment at 170 °C, an inversion of the surface character from hydrophilic to hydrophobic is achieved, which is rather a characteristic of the mechanically exfoliated graphene.<sup>34</sup> We verified this through contact angle measurements with a water droplet, where the average contact angle changed from 68.1° before thermal treatment (inset in Fig. 2a) to 94.8° (inset in Fig. 2b). The thermal treatment is expected to partially remove water and some of the polar functional groups situated at the extreme surface which favor water wetting.<sup>29</sup> Fig. 2 confirms this statement by the deconvolution of the C1s peak of XPS measurements. By heating graphene in vacuum, the amount of carbon-oxygen species such as C-O (~ 286.5 eV) and O-C=O (~ 289 eV) is seen reduced in comparison to the as-received graphene, as well as the C-C or C-H peaks (~ 286 eV) from organic impurities.<sup>35</sup>

Beyond T<sub>PA</sub>=170 °C, significant changes in the graphene surface were not observed. This was also verified by XPS and contact angle measurements. Main C-O and carbon contaminants are efficiently already removed at T<sub>PA</sub>=170 °C and produces a significant surface energy modification. Meanwhile, grafted molecules on graphene, such as PMMA, are not removed.

Non-thermal methods have been proposed to efficiently PMMA clean graphene.<sup>36</sup> However it goes beyond the scope of this study.

When using  $T_{PA}=170\text{ }^{\circ}\text{C}$  as temperature of pre-annealing, the microphase ordering of the PS-*b*-PDMS thin film did not confirm significant changes at  $T_{SA}=150\text{ }^{\circ}\text{C}$  ( $\xi = 39\text{ nm}$  for Fig. 1d). In contrast, the result of the self-assembled BCP thin film at  $T_{SA}=280\text{ }^{\circ}\text{C}$  is shown in Fig. 1e. Correlation length value calculations demonstrated a large improvement in self-assembly ( $\xi = 330\text{ nm}$ ), ten times higher than the one obtained in Fig. 1e. In summary, the ordering rate of the BCP is increased with the temperature annealing  $T_{SA}$  when a previous thermal treatment at  $T_{PA}=170\text{ }^{\circ}\text{C}$  is accomplished. Indeed, when increasing the temperature, the activation energy  $\Delta E_a$  of the chain diffusion is reduced. In this way, the equilibrium ordered structure of the BCP thin films is achieved more rapidly,<sup>37</sup> which explains the significant shift in the correlation length observed in Fig. 1f.

## Surface energy modification of the CVD-grown graphene

Graphene surface energy modification allows engineering self-assembly through two effects. On the one hand, self-assembly kinetics is enhanced, as shown in Fig. 1. On the other hand, it offers control over the preferential wetting of graphene by the individual blocks of the BCP.

Indeed, we observed the BCP-graphene interface by TEM in order to experimentally determine the preferential wetting of the blocks. Despite the significant change in the graphene surface energy at  $T_{PA}=170\text{ }^{\circ}\text{C}$ , PDMS maintains wetting graphene at the BCP-graphene interface when  $T_{SA}=150\text{ }^{\circ}\text{C}$  is used to trigger self-assembly (Fig. 3a), which is problematic for lithography applications.

The work of adhesion  $W$  between the graphene surface and one of the polymer blocks is defined as

$$W_{G-P} = \gamma_P(1 + \cos \Theta) \tag{1}$$

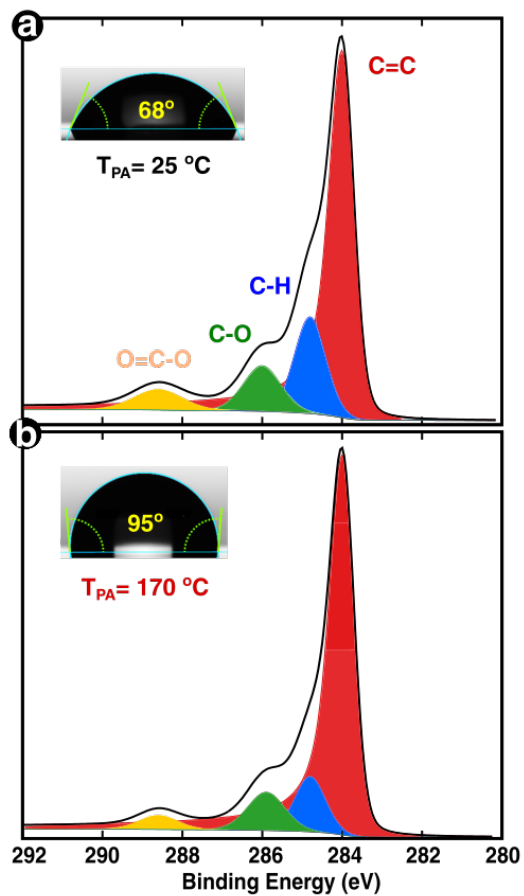


Figure 2: Thermal annealing of graphene to favor self-assembly of PS-*b*-PDMS. Contact angle  $\theta$  and the C1s peak XPS measurement of (a) the as-received CVD-grown graphene and (b) after thermal annealing at  $T_{PA} = 170^\circ\text{C}$ .

where  $\gamma_P$  represents the graphene-polymer interfacial energy and  $\Theta$  is their expected wetting angle on graphene. Using experimental  $\theta$  values (Fig. 2) and the Good and Girifalco model estimation of the interfacial energy,<sup>38</sup> it is possible to estimate the work of adhesion between graphene and PS or PDMS. Calculations of  $W$  are detailed in the Supporting Information. Experimental  $W$  values are displayed in Fig. 3b, as a function of the temperature, as well as Good's model tendency.

The  $W$  values gives important information about the preference wettability of the blocks as a function of the wetting angle. In both contact angles  $\theta$  measured (fig. 2), a lower  $W$  was calculated for the PDMS block. As a result, the PDMS wetting corresponds to the minimal energetic configuration. Clearly, the Good's model shows <sup>S</sup>~~in Fig. 3b~~ that the polymer wetting of graphene is expected to change the graphene wetting at higher temperatures: the PS wettability tends to be energetically more favorable for temperatures higher than 220 °C.

~~Based on the above discussion on wettability of graphene, at higher temperatures~~ **Nevertheless, at higher temperatures,** a much greater vacuum is needed in order to avoid graphene oxidation, sacrificing throughput. Moreover, at ~~higher temperatures than 170 °C~~ **higher than 170 °C,** the graphene surface did not experience important changes in terms of surface energy. These are the reasons why  $T_{PA}$  was limited to 170 °C but rather  $T_{SA}$  was increased up to 280 °C at which the BCP coating protects graphene from oxidation.

At this temperature, we observed that the PS matrix directly wets graphene, which ~~supports the Good's model in Fig. 3b.~~ **presented** Thus, the previous thermal annealing of graphene at  $T_{PA}=170$  °C in vacuum provides a surface energy modification to favor self-assembly kinetics by reducing the C-O species on the surface. On the other hand, a higher  $T_{SA}$  both favors self-assembly **kinetics** and a PS wetting.

We supposed that, when self-assembling at  $T_{SA}=280$  °C, an additional local change of free energy at the BCP-graphene interface could take place, allowing not only a significant increase in the polymer chain mobility, but also a change in the wetting preference.

Thus, thermal surface energy engineering gives a technological solution to self-assemble

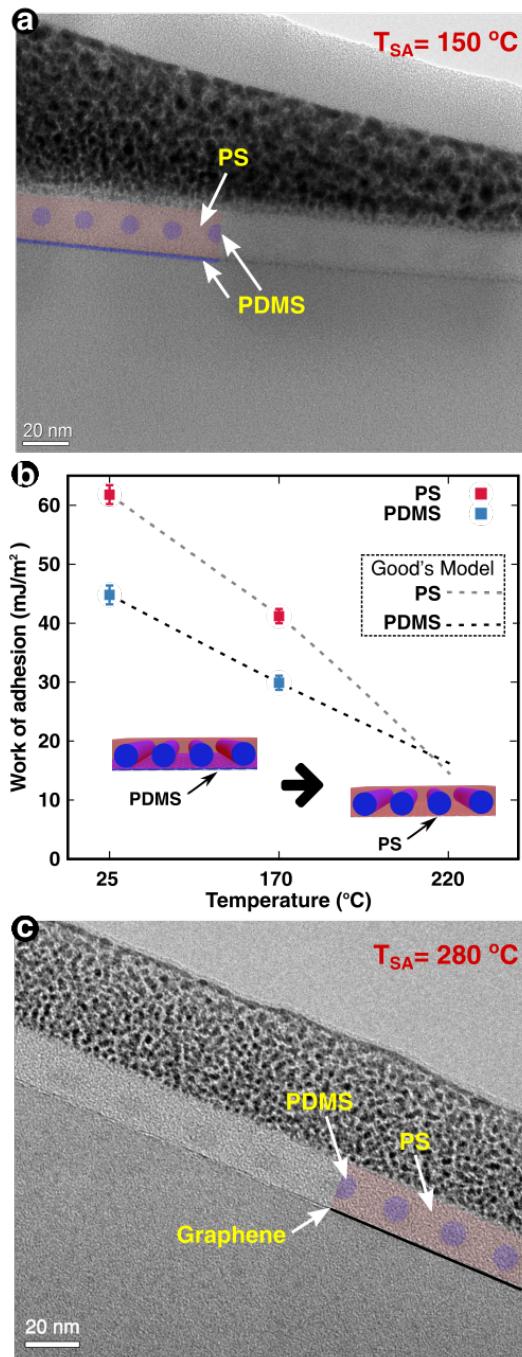


Figure 3: Self-assembly of PS-*b*-PDMS on graphene following a thermal annealing treatment at  $T_{PA}=170\text{ °C}$ . Cross-section TEM images for (a)  $T_{SA}=150\text{ °C}$  and (c)  $T_{SA}=280\text{ °C}$ . (b) Work of adhesion between graphene-polymer interfaces as a function of the temperature. For comparison and to help the reader, the TEM images were partially colored with the observed interfaces. In both cases, the natural period corresponds to 20 nm, as expected.

PS-*b*-PDMS directly on the surface without inducing structural modifications in graphene (Fig. S2). Our method has proven to be more efficient than the usual surface modification by polymer-brushes or other organic molecules as previously proposed,<sup>39</sup> limiting the impact of patterning on graphene properties for device development.

## Dimensional characterization

Self-assembly studies of PS-*b*-PDMS on graphene allows the fabrication of a BCP lithography masks for graphene patterning. Using an oxygen-based plasma etching <sup>process</sup> developed by our research group and reported elsewhere,<sup>40</sup> it is possible to accurately reproduce the BCP periodical nanostructures on graphene and produce GNR arrays on large surfaces. At the same time, as the establishment of a fabrication procedure allows to investigate the properties of GNRs, a proper characterization of GNRs under larger areas is needed. It is important to emphasize the fact that all steps developed here aim at clean-room fabrication.

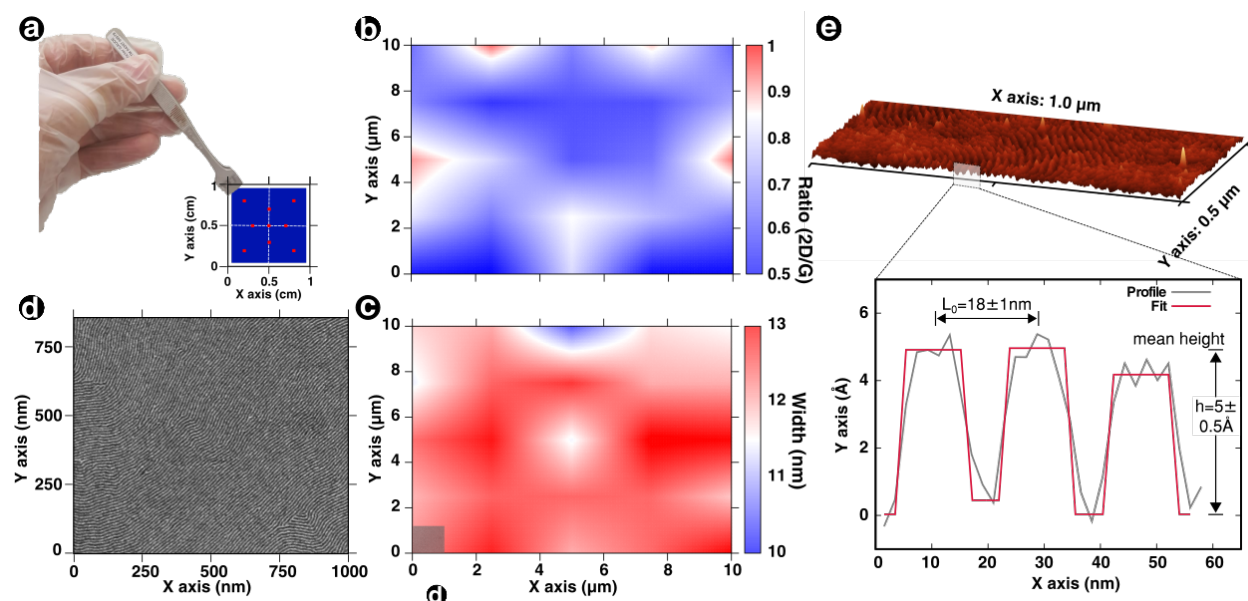


Figure 4: (a) 1 cm<sup>2</sup> sample of GNR arrays on SiO<sub>2</sub>. Mapping of GNRs with Raman spectra on a 100 μm<sup>2</sup> area. (a) I(2D/G) ratio intensities and (b) the GNR average widths calculated from the I(D/G) ratio intensities and the Caçado relation.<sup>41</sup> The experiments were performed with a green laser  $\lambda = 532\text{nm}$ . (d) Top-view SEM image GNRs on a 1 μm<sup>2</sup> area. (e) 3D representation of GNRs scanned by AFM. Inset: dimensional characterization of GNRs.



Raman mapping of patterned graphene performed on  $100 \mu\text{m}^2$  areas are shown in Fig. 4b. Raman spectroscopy has gained popularity in the quantification of defects in nanometer-sized graphene objects. Indeed, the disorder D peak originating from scattering at the ribbon edges, is introduced during graphene etching.<sup>42</sup> The GNR edges are interpreted as an amount of  $Csp^3$  border (one-dimensional defect) with respect to the total  $Csp^2$  crystalline area. From this model, the average distance between defects  $L_D$  can be extracted.<sup>43</sup> The Cançado relation, with  $\lambda_L$  the excitation laser wavelength used during Raman measurements, can be written as:

$$L_D^2(\text{nm}^2) = (1.8 \times 10^{-9})\lambda_L^4 \frac{I_D}{I_G}^{-1} \quad (2)$$

allowing to quantify  $L_D$  from the integrated intensities of the D and G peaks  $I_D$  and  $I_G$  respectively.<sup>41</sup> As the measured surface has a homogeneous matrix of GNRs, with a periodic width, the distance between defects is taken as the average GNR width ( $w$ ). For a good approximation, it is supposed that the point defects are only present at the GNR edges and that the GNR array is composed of a mix of armchair (AGNR) and zigzag (ZGNR) edge chiralities.<sup>44</sup> Fig. 4c shows the 2D distribution of the calculated GNR widths in a  $100 \mu\text{m}^2$  area. From this, the GNR average width was deduced to  $12 \pm 1$  nm.

Moreover, the  $I_{2D}/I_G$  intensity ratios on the same surface were calculated and displayed in fig. 4b, where average ratios are measured at 0.6. As the 2D-peak depends on the illuminated area, it is expected to observe a decrease of the  $I_{2D}/I_G$  ratio corresponding to the decrease of the amount of graphene.<sup>45</sup> Then, it proves that the increase of the  $I_D/I_G$  ratio comes mainly from graphene patterning on the measured area. These results were generalized to larger areas as great as  $1 \text{ cm}^2$  (Fig. 4a) and then used for electrical characterization or further studies.

<sup>t</sup>  
 Additional characterizations included AFM and SEM for the dimensional characterization of GNRs. Fig. 4d shows a top view SEM image on a  $1 \mu\text{m}^2$  area of structured graphene after plasma etching and BCP mask stripping. Then again, Fig. 4e shows a 3D representation

of a GNR array on the same area. The average GNR height and width are  $0.5 \pm 0.1$  nm and  $10.5 \pm 0.5$  nm, respectively. The height and width distributions were constructed by sampling 50 profiles in the image at each point in Fig. 4a and by fitting the positive step to calculate the height and width of the GNRs.

## GNR-FET device

A transition of the electrical regime from its semi-metallic nature to a semiconductor behavior through bandgap opening via structuration is expected.<sup>46</sup> Moreover, this transition could confirm the effective graphene patterning using the BCP mask. Therefore, electrical characterizations were carried out as a complementary characterization method as well as a technological application of high- $\chi$  BCP thin films and nanostructured graphene.

The quality of the GNRs after fabrication was a major concern as the very reactive edges play a fundamental role in the electronic characteristics of the GNRs.<sup>47</sup> The main issue using classical photolithography for contact deposition is the direct redeposit of photoresist after GNR cleaning.<sup>40</sup> The photolithography transferred pattern method (PTP method represented in Fig. S3a) provides an alternative solution to directly deposit metallic contacts on GNRs without photoresist spin-coating.<sup>48</sup>

Electrical tests were performed using the PTP method of contacts deposition on GNR arrays. As represented in Fig. 5a, back-gated FET were fabricated from the GNR arrays (Fig. S3b). The three-terminal device consisted in a GNR array channel with Au source and drain contacts, having a channel length of  $2 \mu\text{m}$ . Our GNR arrays connected the source and the drain electrodes (Fig. S3c). Of 20 devices tested, 8 devices were successfully working. It shows the effectiveness of our method on patterning graphene over large surfaces. Taking into consideration the orientation distribution of the GNR arrays on the surface, the dysfunctional transistors were most probably due to the source and drain not being connected.

Fig. 5b shows representative current-voltage (I-V) characteristics of the FET based on unpatterned graphene sheets (blue curve) and GNRs (red curve), measured at  $V_G = 0$  V (FET

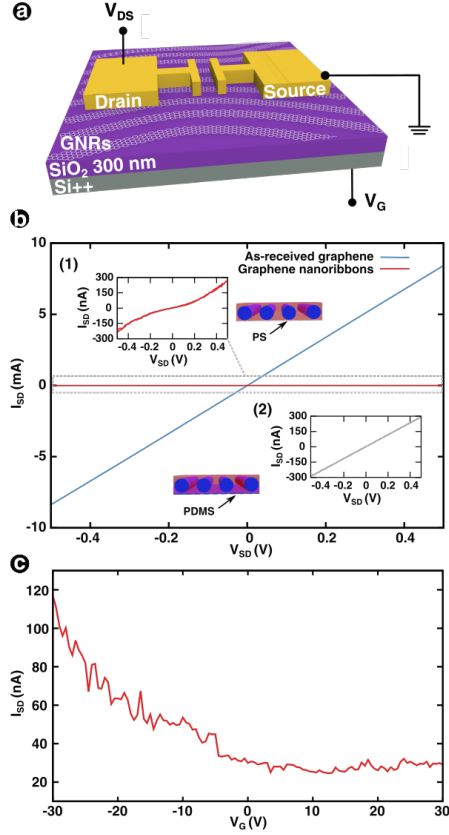


Figure 5: Electrical characteristics with Au contacts by photolithography transferred patterns. (a) Schematic representation of the back-gated FET: 100-nm thick Au contacts with length channel dimensions of  $2 \mu\text{m}$ . Representative current-voltage ( $I$ - $V$ ) characteristics at  $V_G = 0$  V of the as-received CVD-grown graphene and (1) the patterned graphene for comparison; (2) the case when interfacial PDMS impedes patterning. (d) Transfer characteristic curve at  $V_{DS} = 0.2$  V, of the patterned graphene. Calculated  $I_{on}/I_{off}$  was  $\sim 3.7$ .

device shown in Fig. S3b). When the graphene sheet is used as the conducting channel of the FETs, we observed a typical metallic behavior, as predicted by the theory,<sup>49</sup> with a linear relationship of the current flowing through the channels across the  $V_{SD}$  voltage range. Next, measuring electrical response of the FET with GNR arrays, the current measured in a similar range of  $V_{SD}$  exhibited a substantial decrease of 5 orders of magnitude with a highly nonlinear I-V relationship (Fig. 5b-1). This indicates the emergence of a semiconductor behavior (or band gap opening) due to the lateral confinement effect resulting from an effective modification of graphene into GNRs.

The  $I_{DS} - V_{DS}$  characteristics of Fig. 5b-1 became nonlinear in the GNR FETs regardless of the applied gate voltages, without significant hysteresis at ambient conditions. Vacuum and low temperature conditions were necessary in previous reports to avoid hysteresis effects.<sup>17</sup> It could be explained by a sensitivity to environment from the related materials. This clearly reflects once again the high structural quality and stability of the GNR arrays and corroborates our fabrication method, i. e., block copolymer lithography. As a gate voltage was applied, an important modulation of the current is observed due to the movement of the Fermi level.

The semiconductor behavior of the GNRs was also demonstrated by the behavior of the transfer characteristic curve (i.e., the source-drain current  $I_{SD}$  as a function of the gate voltage  $V_G$ ) obtained at ambient conditions, as shown in Fig. 5c. One of the parameters allowing to qualify the FET performance is the ratio between the current at the FET open state  $I_{on}$  and the current at the closed state  $I_{off}$ . The  $I_{on}/I_{off}$  ratio must be as large as possible in order to obtain a clear characteristic between the two states. The simplest and most widespread way used to determine the  $I_{on}$  and  $I_{off}$  values is to take the maximum current value on Fig. 5c ( $I_{on} \sim 112$  nA) and its minimum value ( $I_{off} \sim 30$  nA). From Fig. 5c, the  $I_{on}/I_{off}$  ratio was calculated to be around 3.7. This result confirms the GNR theory, indicating effective patterning of graphene using BCP self-assembly. If any bandgap between the valence and conduction bands is opened up in graphene, this discontinuity by definition

compensates the metal-graphene Schottky barrier.<sup>50</sup> The off current  $I_{off}$  exponentially scales as  $\exp(-q\phi_{barrier}/k_B T)$ , then the bandgap opening value  $E_g$  induced by the patterning of the graphene behaves as an Arrhenius equation,<sup>51,52</sup>

$$\frac{I_{on}}{I_{off}} \propto e^{\left(\frac{E_g}{2k_B T}\right)} \quad (3)$$

where  $I_{on}$  and  $I_{off}$  are respectively the maximum and the minimum current measured in the transfer characteristics curve,  $q$  is the electron charge,  $\phi_{barrier}$  is the Schottky barrier height,  $E_g$  is the energy gap in eV,  $k_B$  is Boltzmann constant and  $T$  is the temperature at which the experiment was performed. This method easily links electrical properties with the intrinsic material property  $E_g$ . Then, from Fig. 5c, the energy bandgap in GNRs was calculated to 70 meV. This value presents the average bandgap from the 8 functional FETs measured.

Even so, the bandgap values found are still weak to develop fast logic FETs: upto hundredths of meV in order to develop an ultrafast logic electronics.<sup>53</sup> Important efforts must now be focused on improving FET performance. This could be possible through better FET design or even GNR edges tailoring in order to improve the transfer characteristics of devices. Additional distribution of the  $I_{on}/I_{off}$  ratio on 8 different measurements is shown in Fig. S3d, with a 3.7 average ratio and the bandgap values calculated at 70 meV using eq. 3. The fabricated devices had characteristics similar to most of literature GNR-based devices (table S1) when a lithography mask was used.

Making the same device where the PDMS wets graphene (PS-*b*-PDMS thin film morphology shown in fig. 3a), an ohmic regime behavior with high current values (hundredths of microamperes) was measured (Fig. 5b-2), This confirms that the PDMS wetting layer effectively obstructs the selective etching of graphene while a probable diffusion of electron acceptors from oxygen plasma causes a decrease in electron mobility. This tuning of the electrical properties by the periodical exposition of pristine graphene to the CF<sub>4</sub> plasma was previously reported.<sup>54</sup>

## Conclusions

The self-assembly of a PS-*b*-PDMS BCP 16kg/mol was studied to obtain a  $\sim 11$  nm resolution hard mask for graphene patterning. Best self-assembly results ( $\xi > 300$  nm) were obtained with direct spin-coating over CVD-grown graphene by annealing at higher temperatures ( $T_{SA} = 280^\circ\text{C}$ ). At the same time, based on work of adhesion calculations, a preferential wetting of the PS-*b*-PDMS thin film was achieved (PS on graphene) which allowed a successful pattern transfer to graphene. Patterned graphene was characterized on large surfaces using Raman mapping. Graphene nanoribbon (GNR) arrays with channel widths of  $11 \pm 1$  nm were measured on large areas. Contact deposition was achieved by an innovative photolithography pattern transfer method. This procedure avoids direct photoresist deposition on the GNRs for electrical characterization of the fabricated structures. The highly nonlinear I-V relationship indicated the emergence of a semiconductor behavior (or band gap widening) through lateral confinement effect in the GNRs. Average  $I_{on}/I_{off}$  was  $\sim 3.7$  with a corresponding bandgap of 70 meV. The lithography procedure developed in this investigation could also be generalized to fabricate different graphene nanostructures such as graphene nanomeshes or quantum dots that could be considered for other applications in functional devices.

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## Supporting Information Available

The following files are available free of charge.

- Suppinfo: additional figures, and methods including detailed work of adhesion calculations, photolithography transfer pattern and Raman analysis. Device images, statistics and literature positioning is also included.

This material is available free of charge via the Internet at <http://pubs.acs.org/>.

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# Graphical TOC Entry

