Low cost low sampling noise UWB Chipless RFID reader

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Abstract — This article presents a potentially low cost low sampling noise reader for the UWB chipless RFID technology. The reader has been designed around the time equivalent approach to reduce its realization cost. A significant effort has been spent for the optimization of the schematic and of the layout to obtain a system with a very low sampling noise. This latest aspect is very important in order to realize a reader for the UWB RFID chipless technology. It has been demonstrated how, with an accurate design, is possible to realize a low cost equivalent time acquisition system with performance comparable with a high cost real time acquisition system. It has been possible to acquire, with a discrete precision, an UWB impulse with a pulse width of only 70 ps.

Index Terms — Chipless RFID, reader, jitter, sampli ng noise.

I. INTRODUCTION

The RFID (Radio Frequency Identification) is one of the most widespread technology in the world concerning the identification of objects and animals. Compared to RFID technology, bar-code is widely more employed for the identification of items. This is because of its lower cost in terms of the realization of the tags and readers. In fact today the realization cost of a bar-code tag is nothing compared to a classical UHF RFID tag, characterized by the presence of a chip, that is around 5-10c€ [1].

Recently a new kind of RFID tag, characterized by the absence of the chip, has been developing. Indeed the chip and the price of the chip's report on the antenna are the most expensive part of a conventional RFID tag. This new kind of tag, called chipless RFID tag, is intended to play an important role in the future for the identification of items [1].

The chipless RFID tag works in UWB, which means in a free band between 3.1 and 10.6 GHz. Each tag needs a suitable reader to collect the information from it. A reader for chipless tag, to be compliant with the European (ETSI) and North American (FCC) regulations in terms of UWB power, sends to the reading tag an UWB impulse, in turn the tag reflects the incoming signal shaping it. The reader can decode the ID of the tag analyzing the shape of the backscattered signal [2].

Today there is not chipless RFID reader available in commerce, so to allow the diffusion of the chipless RFID technology a cheap reader needs to be developed.

A chipless RFID reader based on the equivalent time principle, in order to decrease its realization cost, has been designed. Subsequently, major improvements have been done in order to decrease dramatically its sampling noise. For this, a second reader architecture has been designed. In fact, to acquire the response from the tag the reader converts it in digital. The AD conversion implies a sampling process of the measuring signal. As we will study more accurately in the third section, because of the jitter of some signals inside of the system, this sampling process is affected by noise, which affects especially the component of the measuring signal at higher frequencies (that is to say the fast variations of the signal in time). In addition, the impulse generator used for chipless technology presents lower power at higher frequencies. Thus, reducing the sampling noise of the reader is fundamental to guarantee suitable performance for reading chipless RFID tag.

This paper is structured as follow. The first section describes the equivalent time principle and put it in relation with the block diagram of the first version of the chipless RFID reader. The second section describes some results of measure performed with the reader presented in the previous section. The third one introduces the second reader version, designed in order to decrease its sampling noise, and presents the same measures realized with the previous reader.

II. EQUIVALENT TIME PRINCIPLE AND BLOCK DIAGRAM OF THE FIRST DESIGNED READER

The equivalent time approach is based on the stationary character of the measuring signal. In case of chipless RFID tags this signal is the sign of the tag, which is the reflected signal by the tag, after an interrogation from the reader [1].

In the equivalent time approach the reader sends a discrete number of UWB impulses to the tag and, for each backscattered signal, it acquires only few points. For each receiving signal the sampling frequency of the reader is very low, compared with the UWB, and the acquisition process is shifted in time of few picoseconds. After the end of the acquisition process the reader rearranges all the acquired samples, in order to reconstruct the backscattered signal from the tag, and so to identify its ID [2].

The Fig. 1 shows the block diagram of our reader. It is composed by two different PCBs connected through a VITA 57.1 MC LPC connector. The control unit is entrusted by a FPGA device, the Spartan 6 from Xilinx, in its SP601 evaluation board. The smallest PCB on top represents the RF part and is basically composed by a sample and hold amplifier, an ADC and a delay generator.

The reader samples each UWB backscattered signal with a very low frequency, 67 MHz, thanks to the high performance sample and hold amplifier which has an input bandwidth of 10GHz. It is capable to sample an UWB signal and maintain

its output constant during an entire clock cycle in order to let the following ADC to digitize it. Obviously the ADC, presenting a constant input for an entire clock cycle, is not affected by sampling noise. For each backscattered signal the reader takes only few points. Thanks to the delay generator the sampling clock is delayed of 10 ps for each receiving signal. It allows the system to obtain an equivalent time sampling rate of 100 GSa/s. The impulse generator is triggered by the low sampling frequency of the reader. Thanks to it we can tune the delay generator in order to acquire few samples for each receiving pulse, at known and controlled positions, except for the presence of any jitter which can disturb the acquisition.

III. MEASUREMENT RESULTS FOR THE FIRST DESIGNED READER

The sampling noise of a chipless RFID reader is correlated with the jitter of some of its signals, which provoke the acquisition of some samples of the input in an incorrect position in time. Later, in the reconstruction process, it will affect the correctness of the reconstructed signal. To clarify the concept of sampling noise we can take as example an ADC. Assuming the converter performing the sampling, of its analog input, at each clock event, represented by its rising edge, and supposing it affected by jitter. Hence the converter will sample, and therefore convert, a value of tension taken in a wrong and unknown position on time. Then, in the digital world, the incoming signal will be reconstructed assuming a sample period constant and equal to the nominal clock period. Since that at each point in time will be coincided a digital value, of a sample, taken not exactly at that position in time, from the ADC, but at a different one because of the jitter that affects the clock. This means the digital value assigned at that point is wrong. The mistake will be higher as higher is the slew rate of the incoming signal. For a harmonic signal the slew rate is directly proportional to its frequency and amplitude. Thus the problem of sampling noise is more significant as the frequency increases. Supposing a Gaussian jitter, the following equation gives the relation between the jitter and the sampling noise [4].

$$\sigma = \sqrt{2}\sigma \ .$$

Where σ is the deviation standard of the jitter and σ is the same but of the error introduced on the acquired signal. The signal to be sampled is a harmonic with amplitude A and frequency *f*.

The reader has a bistatic configuration where, through an UWB transmitting antenna, the UWB impulse is sent to the tag and its response is captured by another UWB antenna. For our measures the two antennas have been disconnected. The output of the reader, represented by the output of the impulse generator, has been directly connected with its input, the input of the LNA amplifier, through the interposition of an attenuator, and some acquisition has been performed.

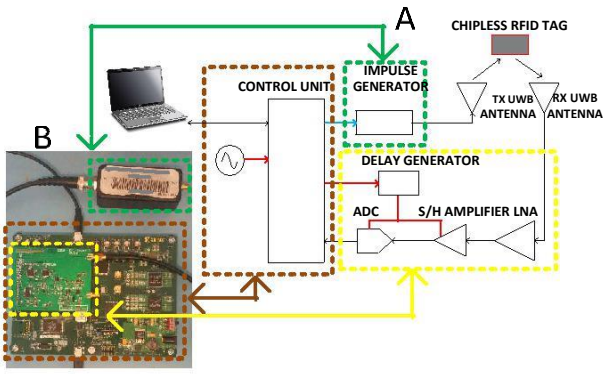

Fig. 1. Block diagram(A) and photo(B) of the first version of the realized reader for chipless RFID applications. The control unit is entrusted on a FPGA Xilinx spartan 6 on the evaluation board SP601. The RF part is the smallest PCB on top of the SP601.

To appreciate the effect of the sampling noise of the acquired response and the equivalent time principle, a comparison between the UWB impulse, measured with a high performance DSO, and the input of the ADC of the reader is reported in Fig. 2.

The duration of the impulse, less than 1 ns, is very low if compared with the clock period, 15ns, of the reader. Therefore, for each impulse sent by the impulse generator, at most one point of it is acquired by the system. This is the reason why, in fig. 2, the shape of the measured input of the ADC of the reader can follow the shape of the impulse acquired with the DSO. Comparing the two curves is clear that the acquisition made with our reader is affected by sampling noise. This is especially evident in the rising and falling edges of the impulse, where its slew rate is bigger.

IV. LOW JITTER READER DESIGN AND MEASUREMENT RESULTS

There are three signals that establish the position in time of each sampling event, for the sample and hold amplifier, compared with the signal coming from the tag. These three

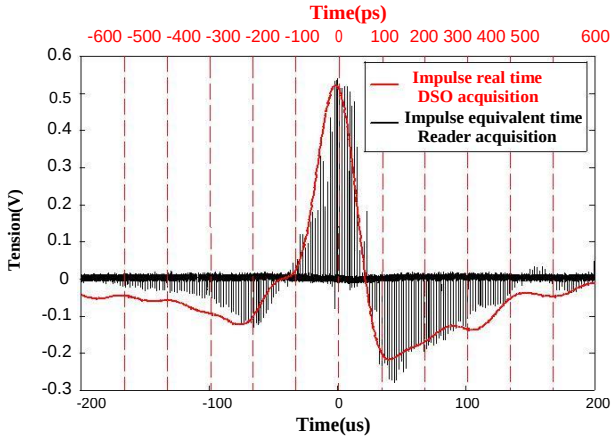

Fig. 2. Comparison between the attenuated output of the pulse generator, measured with a DSO, and the input of the ADC of the first reader in order to appreciate the sampling noise of the system and the equivalent time algorithm.

signals are: the rising edge of the clock of the sample and hold amplifier, the trigger signal of the impulse generator and the delay imposed by the delay generator. Except for the latest one, the other two fundamental signals for the sampling noise come from the FPGA; which is a devise not designed to provide signals with an extremely low jitter[5].

To decrease dramatically the sampling noise, two design choices have been implemented on the second developed reader. The first one was the design of a multi-clock system where the ultra-low jitter clock generator, for the RF board, is placed directly on that board. Moreover it is independent from the clock used for the FPGA that is located on the evaluation board SP601. The second choice was to keep the connection between the trigger signal, for the impulse generator, and the FPGA but getting the rising edge instant of the trigger signal, which commands the impulse generator, independent from the FPGA. It can be obtained with a high performance low jitter AND gate placed on the RF board, where in one input is presented the external clock located on that board, which means a low jitter signal, and in the other one the signal that comes from the FPGA characterized by an high jitter.

The Fig. 3 shows the new reader version. We can recognize the ultra-low jitter clock generator presented on the RF board and the AND gate. In order to ensure a low jitter system, the RF PCB has been carefully designed in order to optimize the signal integrity. Moreover have been chosen components characterized by ultra-low jitter with suitable digital standards. The measure of the period jitter of the sampling clock, of the sample and hold amplifier, for both the readers has been performed. For first version of the reader the jitter presents a standard deviation of 7.34ps and a maximum of 115.7ps meanwhile it is of only 2.45ps in the latest version with a maximum of only 16.31ps over 1.5k cycles measured.

In Fig. 4 is reported the same measure of Fig. 2 performed with the second reader. Clearly the second reader presents a much lower sampling noise especially where the slew rate is bigger, which is in the rising and falling edges of the impulse.

Indeed the width of the UWB impulse is of only 70 ps.

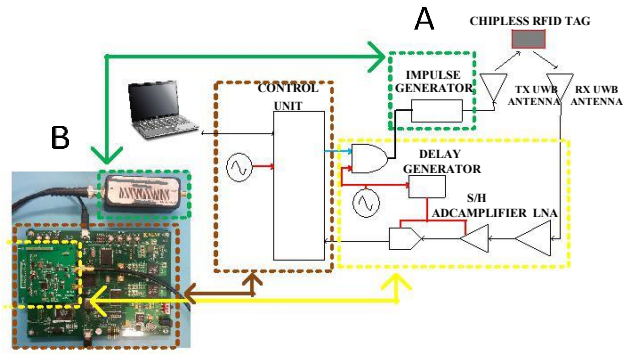

Fig. 3. Block diagram(A) and photo(B) of the second realized reader for chipless RFID tags. The control unit is entrusted on a FPGA Xilinx spartan 6 on the evaluation board SP601. The RF part is the smallest PCB on top of the SP601. The RF PCB presents a second clock generator and an ultra-low jitter AND gate to decrease the sampling noise of the system.

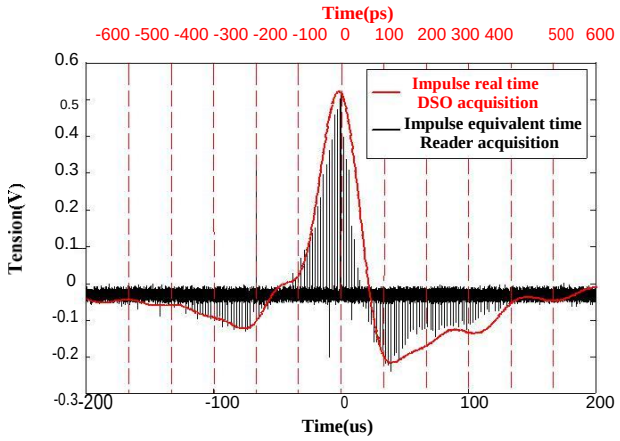

Fig. 4. Comparison between the attenuated output of the pulse generator, measured with a DSO, and the input of the ADC of the second reader in order to appreciate the sampling noise of the system and the equivalent time algorithm.

Besides, the already low sampling noise may steel decreased through an averaging of different acquisitions.

The low sampling noise of this new reader makes it suitable to be used as chipless RFID reader and it is largely affordable. Indeed, excluding the two antennas, its realization cost is about 2000€ where the most expensive components are the impulse generator (900€) and the sample and hold am plifier (700€). The two presented reader have approximately the same realization cost but a significant difference in terms of performance.

V. CONCLUSION

In this article has been shown how to design a high performance low cost reader for chipless RFID applications. It has been shown how to decrease the sampling noise, which is vital in a time equivalent approach system for UWB, through the correct design of the reader.

VI. REFERENCES

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