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Evolution of bulk c-Si properties during the processing of GaP/c-Si heterojunction cell

Renaud Varache[a], Maxime Darnon[b], Médéric Descazeaux[a], Mickael Martin[b], Thierry Baron[b], Delfina Muñoz[a]

[a] *CEA-INES, LITEN, 50 Avenue du Lac Léman, F-73375 Le Bourget-du-Lac, France*
[b] *Univ. Grenoble Alpes , CNRS, CEA-Leti Minatec, LTM, F-38054 Grenoble Cedex, France*

Abstract

One of the limitations of current amorphous silicon/crystalline silicon heterojunction solar cells are optical losses in the amorphous silicon (a-Si:H) layers that limit the short circuit current. In this work, we propose to replace amorphous silicon layers by a thin crystalline gallium phosphide (GaP) layer in heterojunctions solar cells. We show that the better transparency of GaP compared to a-Si:H promises gain in the UV region. However, the annealing in the MOCVD chamber before GaP growth that is necessary for high quality GaP epitaxial growth degrades the bulk silicon minority carrier lifetime. This degradation is attributed to fast diffusing species and can be overcome by a gettering process.

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Keywords: gallium phosphide ; heterojunction ; silicon ; solar cell ; MOCVD

1. Introduction

Heterojunctions silicon-based solar cells have been studied for years [1-6,7]. There has been a regain of interest in these structures with the development and commercialization of so-called HIT solar cells by the Japanese company Panasonic [8]. Such solar cells have shown record efficiencies of 24.7% with front contacts and 25.6% with back contacts thanks to the extremely good passivation of the silicon surface by intrinsic hydrogenated amorphous silicon (a-Si:H) layers and to the large band-gap of a-Si:H [9]. However, absorption in the a-Si:H layer limits the efficiency in the UV region. To leverage the progresses made in heterojunction solar cells while improving the efficiency in the UV, it would be interesting to integrate new materials as front emitter with a higher transparency than a-Si:H.

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Gallium Phosphide (GaP) has a lattice constant of 5.4906 Å that is close to the one of c-Si (5.4307 Å), making it candidate for epitaxial growth on silicon [10]. In addition, GaP has a bandgap energy of 2.26 eV at 300 K and is therefore transparent to photons with a wavelength above 545 nm [2,11-13].

Some groups have investigated GaP as a material for heterojunctions or as a window layer on silicon solar cells [1,2,11,12,14]. Shahai and Milnes have computed several heterojunctions solar cells including a 5 µm- and a 250 µm-thick GaP layer on silicon. They estimate the efficiency around 10%, close to the efficiency of the Silicon homojunction they computed. They anticipate though a loss in photogeneration because the optical absorption edge in the UV is sharper for GaP than for c-Si [2]. Katoda and Kishi reported the first GaP/c-Si heterojunction solar cell with an open circuit voltage (V_{OC}) of 660 mV and an efficiency of 1.7% [11]. Landis et al. used GaP grown by MOCVD (Molecular Organic Chemical Vapor Deposition) as a window layer on an homojunction silicon solar cell but also reported the GaP/c-Si heterojunction solar cell results in their paper. They obtain a V_{OC} of 603 mV, which is lower than the one of their homojunction silicon solar cell. They showed that the GaP heterojunction provided excellent passivation but was significantly absorbing in the short wavelengths end of the spectrum [12]. Huang et al. used LPE (Liquid Phase Epitaxy) to form multijunctions GaP/c-Si solar cells and also report a GaP/c-Si heterojunction solar cell with a V_{OC} of 508 mV and an efficiency of 8%.

Recent progresses have been published on GaP growth on silicon. On nominal c-Si <100> wafers, it has been demonstrated that antiphase boundary defects (APD) could be confined to the first 40 nm [15]. By choosing a slight miscut angle and proper growth initiation, the volume of the APDs could be also minimized [16].

In this paper, we propose to use GaP as a replacement of amorphous silicon on the front side of heterojunction silicon solar cells. A 10 nm-thick layer of GaP is grown by epitaxy on nominal <100> silicon by Metal Organic Chemical Vapor Deposition (MOCVD), and the integration flow of a-Si:H/c-Si heterojunction solar cells is used to build a solar cell with a GaP/c-Si heterojunction. We will first discuss the best structures and the limitation of c-GaP/c-Si heterojunction solar cells, and we will discuss then the origin of the limitations.

2. Experimental setup

The proposed structure of GaP/c-Si heterojunction solar cell consists of a p- or n-type crystalline silicon base with a n-type GaP front layer and an a-Si:H (intrinsic and p-type) back layer. For p-type base, the structure has a front emitter while for n-type base the structure has a back emitter. Each surface is covered then with a 70 nm-thick indium tin oxide (ITO) transparent electrode. The back side electrode is a blank silver sheet while the front side electrode is made of screen-printed silver paste grid with one central bus bar and 25 fingers covering an active area of 25 cm^2. Reference solar cells with an intrinsic and n-type a-Si:H front emitter are also used for comparison. The c-GaP growth is performed in a Metal Organic Chemical Vapor Deposition (MOCVD) tool from Applied Material operating on 300 mm silicon wafers. Before the growth, the substrate is deoxidized using a Siconi dry process (NH_3/NF_3 remote plasma) in a separate chamber. Then, the wafer is transferred under vacuum to the MOCVD chamber were it is annealed before the actual GaP growth. Silicon diffusion in the GaP results in an n-type doping of the GaP. The complete process flow for the reference a-Si:H/c-Si and for the c-Si/c-GaP heterojunction solar cells is depicted in Figure 1.

The spectral response is determined using a Spequest system. A broadband light source is first monochromatized between 300 nm and 1300 nm with a step size of 10 nm and chopped at 30 Hz. It shines on the solar cell while the short circuit current is measured with a lock-in amplifier. The source intensity as well as the reflected light are monitored with CCD detectors to extract the external and internal quantum efficiency. The minority carrier lifetime is measured with a Sinton WCT120 in Quasi Steady State Photoconductance (QSSPC) or in transient mode with a flash duration of 1 s or 1/64 s, respectively.

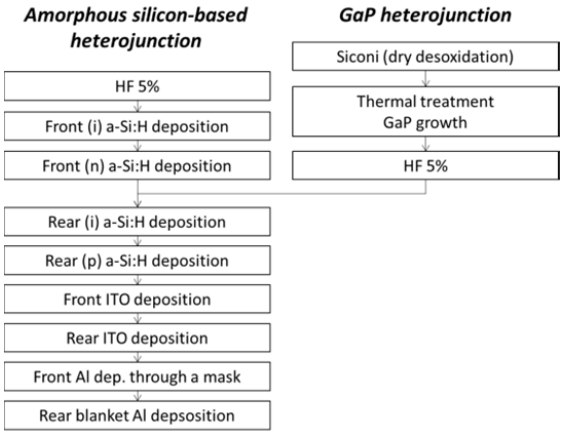

Fig. 1. Process flow used for solar cells fabrication.

3. Experimental results

3.1. Observation of silicon substrate degradation

The Internal Quantum Efficiencies measured on finished cells are shown on figure 2. Different solar cells structures with a front (p-type silicon substrate) and a rear (n-type Si substrate) emitter are reported. First it is worth noticing that the cell with a (n)GaP/(p)c-Si heterojunction has a better response for wavelengths between 400 nm and 600 nm compared to the cell with a (i+n)a-Si:H/(p)c-Si heterojunction (reference cell). This is attributed to the better transparency of GaP compared to amorphous silicon in the UV-region. However, this cell also shows a strong degradation for longer wavelengths compared to the reference cell. This degradation is attributed to a degradation of the bulk silicon properties during the cell fabrication process.

Interestingly, the rear emitter cell with front GaP shows an extremely low IQE over the whole wavelength range, indicating clearly for the first time that GaP does not chemically passivate the c-Si surface. For the largest wavelengths, the IQE reaches the values of the front emitter structure with GaP, confirming the degradation of the bulk properties for both structures with GaP front layer.

These data indicate that the appropriate structures for c-GaP/c-Si based solar cells would be a front emitter structure with GaP on the front surface to beneficiate from the better transparency and from the field effect to minimize losses in the heterojunction. However, for such a structure to compete with standard a-Si:H/c-Si heterojunctions, the degradation of the bulk silicon properties must be understood and overcome.

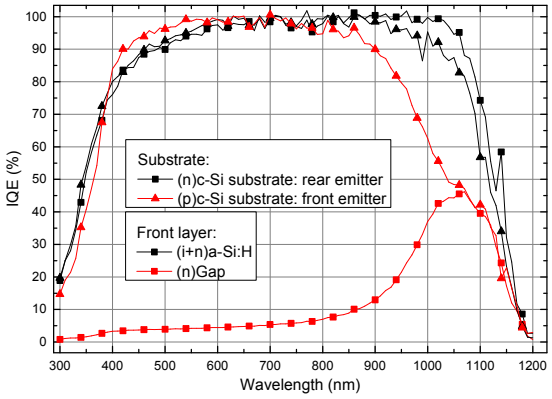

Fig. 2. Internal Quantum Efficiency (IQE) measurement for cells with different structures and thermal treatments.

3.2. Origin of the substrate degradation

To determine the origin of the IQE degradation at the longest wavelengths, we performed minority carrier lifetime measurements on silicon substrates passivated with a-Si:H layers on both sides. Before the a-Si:H deposition, the silicon substrates were treated with specific steps of the process flow for GaP/c-Si fabrication: the wafers were treated or not with the Siconi process and the wafers were annealed or not in the MOCVD chamber. When the wafers were not annealed, they were placed on the MOCVD chuck for few minutes without process. The minority lifetime is reported figure 3.a. This figure clearly shows two populations for the various treatments. In the upper part of the graph, substrates without annealing in the MOCVD chamber present a minority carrier lifetime larger than 1 ms. Therefore the bulk properties of the silicon substrate were not degraded during the treatments. In the lower part of the graph, substrates with annealing in the MOCVD chamber present a minority carrier lifetime below 1 ms. This clearly indicates that the thermal treatment performed in the MOCVD chamber is responsible for the minority carrier lifetime degradation in the bulk silicon. One wafer that sat in the MOCVD chamber were then treated in an oven operated at an identical temperature as the nominal thermal treatment. In this case (not shown here), the minority lifetime was comparable to the one of a silicon substrate that did not see the MOCVD chamber environment before the thermal treatment.

To clarify the role of the thermal treatment on the minority carrier lifetime degradation, we performed additional experiments with various maximum temperature for the thermal treatment (see figure 3.b). In this case too, the silicon wafers were passivated with a-Si:H before minority carrier lifetime measurements. These data clearly show the dramatic effect of the temperature in the MOCVD chamber on the minority carrier lifetime. All these experiments indicate that the minority carrier lifetime degradation is induced by the simultaneous exposition of the silicon to the MOCVD chamber environment and the thermal treatment at a temperature above nominal temperature – 100°C. This tends to indicate that the minority carrier lifetime degradation is due to the contamination of the bulk silicon by species present in the MOCVD chamber that are simultaneously activated by the thermal treatment.

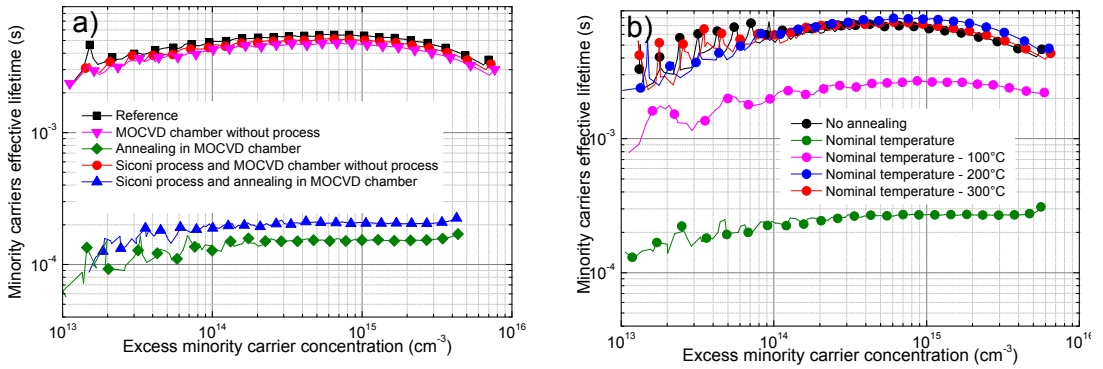

Fig. 3. (a) Minority carrier lifetime measured in p-type 300 mm, 750 µm thick CZ silicon wafers for various treatments in the MOCVD chamber. (b) Minority carrier lifetime measured in p-type 300 mm CZ silicon wafers for various treatments temperature in the MOCVD chamber.

3.3. Analysis of silicon contamination

Additional experiments have been performed to confirm the origin of the minority carrier lifetime degradation. First we exposed a silicon wafer covered by 500 nm of PECVD silicon nitride barrier (each face) to the thermal treatment in the MOCVD chamber. Excellent minority carrier lifetimes are measured (see figure 4.a.), which indicates that the 500 nm-thick Si_3N_4 layer prevents the contaminating species diffusion in the bulk silicon. Second we etched with a diluted KOH solution pieces of silicon extracted from a reference wafer and from a wafer that was annealed in the MOCVD chamber. The amount of silicon removed by the chemical bath was determined with a microbalance. The pieces of silicon were then passivated with a-Si:H on both side and the minority carrier lifetime was measured. The results presented Figure 4.b. show that even after more than 20 µm was removed from each side

of the silicon, the bulk properties of the silicon did not change. This shows that the contaminating species is a fast diffusing species that diffuses more than 20 µm inside the silicon. Finally, TXRF analyses were performed on a sample thermally treated in the MOCVD chamber. As shown table 1, no significant difference is observed except for As and Mg between the reference sample and the thermally treated sample, which indicates that the concentration of the contaminating species is below the detection level. The Mg detection is a measurement artefact from interference with the As line. This was confirmed by ICPMS where Mg concentration was below the detection level of 10^9 cm^{-3}. Arsenic is a dopant for silicon and is not known to be a recombination center.

These various experiments confirm that the minority carrier lifetime degradation is attributed to a contaminating species diffusion from the MOCVD chamber to the sample. The contaminating species has a very low concentration and diffuses across (at least) 20 µm.

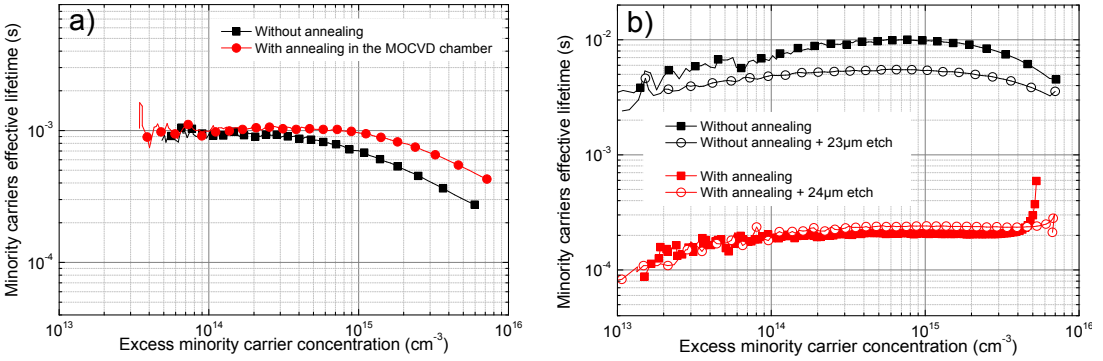

Fig. 4. Minority carrier lifetime measured (a) on p-type 200 mm, 750 µm CZ silicon wafers covered with 500 nm-thick Si_3N_4 with and without annealing in the MOCVD chamber. (b) Minority carrier lifetime measured on p-type 300 mm CZ silicon after etching more than 20 µm from each side of the sample (with and without annealing in the MOCVD chamber)

Table 1. Elemental concentration in cm^{-3} of contamination at the wafer of p-type 300 mm CZ silicon wafer measured by TXRF. *The Mg line interferes with the As line

	Al	As	Au	Br	Ca	Cl	Co	Cr	Cu	Fe
Ref.	< 2E11	5E12	< 5E10	3E11	< 5E11	3E12	< 5E10	< 5E10	< 5E10	< 5E10
Annealed	< 2E11	4E13	< 5E10	< 6E10	< 5E11	1E12	< 5E10	< 5E10	< 5E10	< 5E10
	Ga	In	K	Mg*	Mn	Mo	Na	Ni	P	Pb
Ref.	< 9E10	< 6E10	< 5E11	4E12	< 5E10	< 5E10	< 5E11	< 5E10	< 5E13	< 5E11
Annealed	< 9E10	< 6E10	< 5E11	3E13	< 5E10	< 5E10	< 5E11	< 5E10	< 5E13	< 5E11
	Pt	Ru	S	Ta	Ti	V	W	Zn	Zr	
Ref.	< 5E10	< 5E10	1E13	< 7E10	< 5E10	< 5E10	< 6E10	< 5E10	< 5E11	
Annealed	< 5E10	< 5E10	3E12	< 7E10	< 5E10	< 5E10	< 6E10	< 5E10	< 5E11	

4. Discussion

The major limitation for c-GaP/c-Si heterojunctions solar cells fabrication comes from minority carrier lifetime degradation in the silicon during the surface preparation in the MOCVD chamber. Garcia-Tabares et al. have also observed the degradation of minority carrier lifetime during sample preparation in MOVPE environment.[17, 18] They list three different explanations for this effect. (1) Introduction of intrinsic carrier lifetime killers during the annealing in the chamber. One potential killer element is Zinc that is a known center of recombination. (2) The treatment at high temperatures leads to the formation of crystal defects that eventually become recombination centers. (3) The thermal treatment activates lifetime killing impurities that are already present in the wafer in an inactive state. In our experimental conditions, the lifetime degradation may originate from similar mechanisms. Our experiments rule out the 2nd hypothesis since wafers with identical thermal treatments but not in the MOCVD

chamber do not show significant degradation of the minority lifetime. They also rule out the third hypothesis. Indeed, wafers treated in the MOCVD chamber with a Si_3N_4 barrier would show minority carrier lifetime degradation if the contaminating species were already present inside the silicon. Our experiments show that the first hypothesis is the most valid one. We attributes the bulk degradation to a fast diffusing impurity from the MOCVD chamber in the silicon. The environment in the MOCVD chamber is as clean as possible and no other elements than In, Ga, As, Al, P, H, C and Si have ever been intentionally introduced in the chamber. In addition, contamination measurements by TXRF and VPD-ICPMS on silicon wafers processed in the MOCVD chamber show no significant surface contamination except for As (that was also present on the reference sample but to a lower level). This indicates that the contaminating species is a highly effective center of recombination. Furthermore, the same observation from two different research groups indicates that the contaminating species is a common species in III-V deposition chambers. The exact species is not clearly identified yet.

In their paper, Garcia-Tabares et al. have shown that phosphorous diffusion after the thermal annealing could recover the minority carrier lifetime, which shows that there are technological solutions to overcome the issue of lifetime degradation. We investigated a gettering process to recover the minority carrier lifetime in the bulk silicon. Samples exposed to the thermal treatment in the MOCVD chamber were doped by phosphorous diffusion and chemically etched in diluted KOH. Such processes are known to reduce contaminating species concentration [19]. After this process, the sample was passivated by a-Si:H and the minority carrier lifetime was measured. As shown figure 5, the gettering process recovers the minority carrier lifetime of reference samples while etching only would not recover it. This solution could be used for recovering minority carrier lifetime in the silicon after the full GaP deposition process. However, such solutions would require a detailed development to be performed in conditions compatible with the GaP stability.

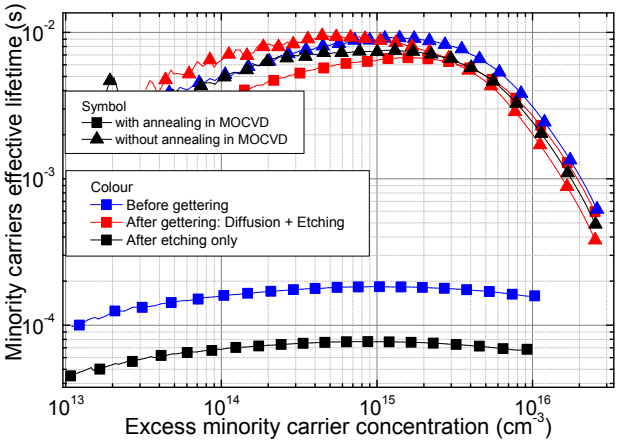

Fig. 5. Minority carrier lifetime for silicon wafers after annealing in the MOCVD chamber, and after phosphorous diffusion and/or etching. The minority carrier lifetime is also reported for a reference wafer without annealing.

5. Conclusion

We have evaluated the potential of GaP as a replacement of a-Si:H in heterojunction solar cells. The spectral response of the cell is improved in the UV region thanks to the lower light absorption of GaP compared to amorphous silicon. We showed that the GaP does not chemically passivate the silicon surface. The best candidate structure is a front emitter c-GaP/c-Si structure to beneficiate from the high transparency and from the field effect between GaP and Si to minimize losses in the heterojunction. With our current process, a strong minority carrier lifetime degradation in the silicon during surface preparation in the MOCVD chamber leads to a decrease in quantum efficiency for long wavelengths. This degradation is attributed to a fast diffusing species with a very low concentration that is common in III-V deposition chambers but that has not been identified yet. If the contaminating species cannot be avoided, solutions like a gettering process have the potential to recover the silicon bulk properties.

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