Anti-phase boundaries–Free GaAs epilayers on “quasi-nominal” Ge-buffered silicon substrates

Y. Bogumilowicz, J. Hartmann, R. Cipro, R. Alcotte, M. Martin, F. Bassani, J. Moeyaert, T. Baron, J. Pin, X. Bao, et al.

► To cite this version:

Y. Bogumilowicz, J. Hartmann, R. Cipro, R. Alcotte, M. Martin, et al.. Anti-phase boundaries–Free GaAs epilayers on “quasi-nominal” Ge-buffered silicon substrates. Applied Physics Letters, 2015, 107 (21), pp.212105. ⟨10.1063/1.4935943⟩. ⟨hal-01991879⟩

HAL Id: hal-01991879

https://hal.univ-grenoble-alpes.fr/hal-01991879v1

Submitted on 20 Dec 2022

APPLIED PHYSICS LETTERS **107**, 212105 (2015)

Anti-phase boundaries–Free GaAs epilayers on "quasi-nominal" Ge-buffered silicon substrates

Y. Bogumilowicz,[1,a)] J. M. Hartmann,[1] R. Cipro,[2] R. Alcotte,[2] M. Martin,[2] F. Bassani,[2]
J. Moeyaert,[2] T. Baron,[2] J. B. Pin,[3] X. Bao,[3] Z. Ye,[3] and E. Sanchez[3]
[1]*Univ. Grenoble Alpes, F-38000 Grenoble, France and CEA, LETI, Minatec Campus,*
F-38054 Grenoble, France
[2]*Univ. Grenoble Alpes, F-38000 Grenoble, France and CNRS, LTM, F-38054 Grenoble, France*
[3]*AMAT, 3050 Bowers Avenue, Santa Clara, California 95054, USA*

(Received 8 September 2015; accepted 5 November 2015; published online 25 November 2015)

We have obtained Anti-Phase Boundary (APB) free GaAs epilayers on "quasi-nominal" (001) silicon substrates, while using a thick germanium strain relaxed buffer between the GaAs layer and the silicon substrate in order to accommodate the 4% lattice mismatch between the two. As silicon (001) substrates always have a small random offcut angle from their nominal surface plane, we call them "quasi-nominal." We have focused on the influence that this small ($\leq 0.5°$) offcut angle has on the GaAs epilayer properties, showing that it greatly influences the density of APBs. On 0.5° offcut substrates, we obtained smooth, slightly tensile strained ($R = 106\%$) GaAs epilayers that were single domain (e.g., without any APB), showing that it is not necessary to use large offcut substrates, typically 4° to 6°, for GaAs epitaxy on silicon. These make the GaAs layers more compatible with the existing silicon manufacturing technology that uses "quasi-nominal" substrates.
[http://dx.doi.org/10.1063/1.4935943]

Significant advances have occurred the last 20 years or so concerning the growth of Si/SiGe heterostructures for microelectronics (high mobility channels for holes, SiGe:B embedded sources and drains, and so on). These advanced epitaxial heterostructures have also been incorporated into high performance integrated circuits that are commercially available. Research is currently focusing on integrating III-V alloys, including GaAs, on silicon. The aim is to combine the advantageous properties of III-Vs (high electron mobility, direct bandgap…) with advanced silicon manufacturing technology. However, growing GaAs on silicon is very challenging. First, there is a large lattice mismatch between silicon and GaAs (a_{GaAs} is 4% larger than a_{Si}) that leads to the introduction of misfit dislocations. Second, there is a thermal expansion difference between silicon and GaAs that can lead to the appearance of cracks in the GaAs layer,[1,2] but this can be solved by limiting the total thickness of the epitaxial III-V layer to less than a few microns. The third difficulty when growing GaAs on nominal (001) surfaces is the existence of anti-phase domains, separated by anti-phase boundaries (APBs).[3–5] As GaAs is a polar material, the epilayers can be seen as a succession of arsenic and gallium monolayers, e.g., an ABAB sequence. ABAB domains and BABA domains will thus coexist when growing on nominal, non-polar substrates due to the nucleation of the film on atomic terraces if there are an odd number of atomic planes between terraces. Obtaining single domain GaAs epitaxial films on silicon has been solved in two ways. First, by using offcut substrates, with a typical offset of 4° to 6° in the $\langle 110 \rangle$ direction,[6–11] in order to promote the formation of bi-atomic steps between terraces and, second, by starting the GaAs growth with an arsenic pre-exposure in order to begin the epitaxy on an arsenic surface.

Some integration schemes have been very recently proposed[12] to grow GaAs on silicon without APBs, but those schemes involve patterning, etching, epitaxial lateral overgrowth, and cannot be compared to an epitaxial growth of a blanket layer, which we will discuss below. In this letter, we have examined the growth of GaAs blanket thick layers on "quasi-nominal" (001) silicon substrates. During the fabrication of silicon substrates, there is always a small offcut angle which can be up to 0.5°, in random crystalline directions, and this is what we mean by "quasi-nominal." We have focused on the influence of these small offcut angles on the properties of GaAs epilayers on silicon, and especially on the presence of APBs in the films, resulting in the elimination of APBs from GaAs epifilms on "quasi-nominal" Si (001) substrates.

The III-V epitaxy has been carried out in an Applied Materials Metal Organic Vapor Phase Epitaxy (MOVPE) equipment that is designed to process 300 mm diameter substrates. Trimethylgallium (TMGa) and tertiarybutylarsine (TBAs) organometallic precursors were used as Ga and As sources, respectively. Ultra-pure hydrogen was used as the carrier gas. Deposition occurred on 775 μm thick 300 mm silicon (001) substrates with an offcut of 0.1°, 0.3°, or 0.5° in the $\langle 110 \rangle$ direction. In our case, this small offcut was intentional, but in practice, nominal (001) substrates are always slightly mis-oriented, whether intentional or not. Prior to III-V epitaxy, a one micron thick Ge strain relaxed buffer layer was grown at 90 Torr using GeH_4 (in a separate group IV epi tool). A low temperature/high temperature deposition strategy was adopted (e.g., 400 °C/650 °C), together with some thermal cycling under H_2 (between 650 °C and 850 °C), in order to minimize the threading dislocation density.[13] This resulted in smooth, slightly tensile-strained Ge layers, with a typical surface Root Mean Square (RMS) roughness of less than 1 nm for a $5 \times 5\ \mu m^2$ Atomic Force

---

[a)] E-mail: yann.bogumilowicz@cea.fr

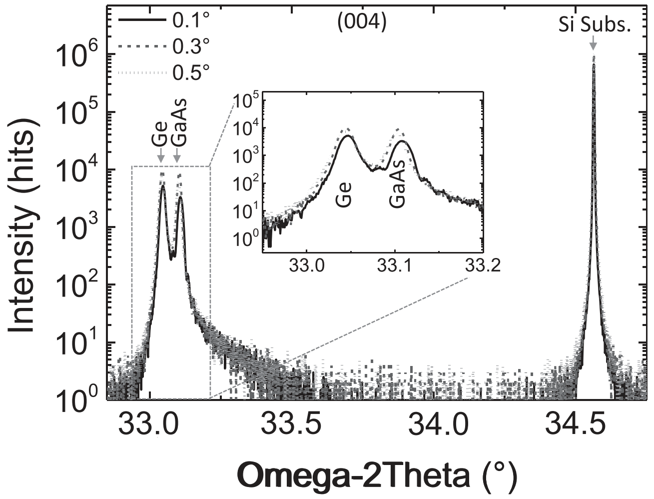
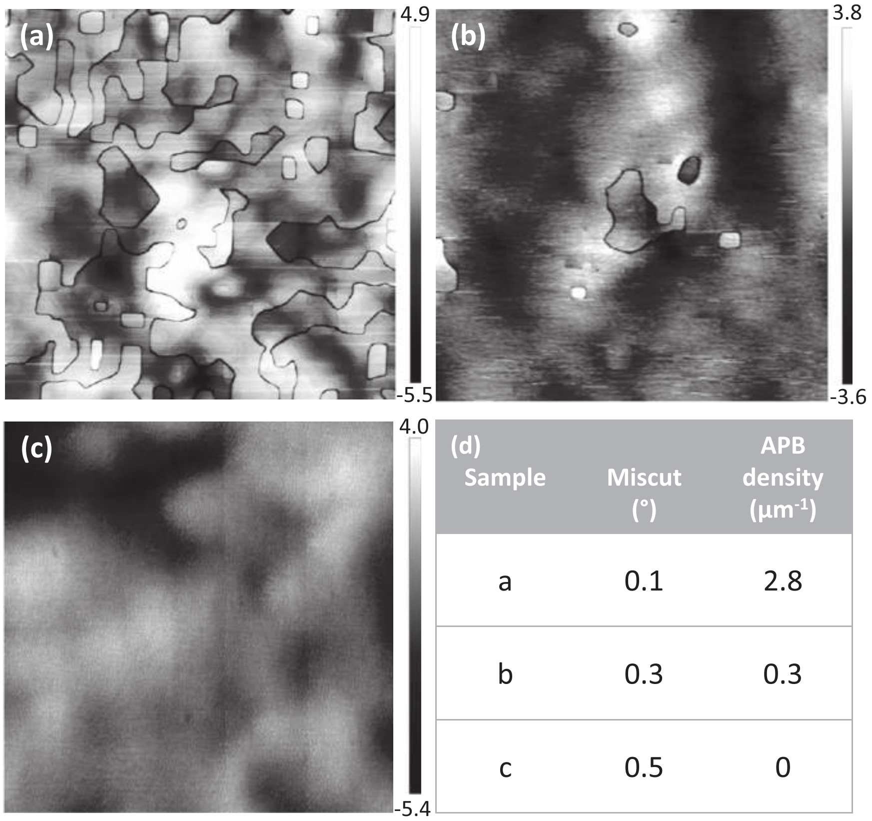


FIG. 1. High resolution, X-ray diffraction profiles around the (004) order (in the triple axis configuration) for a GaAs layer grown on a Ge-buffered silicon substrate with a 0.1° (solid line), 0.3° (dashed line), and 0.5° (dotted line) offcut.

Microscopy (AFM) image. The threading dislocation density in these Ge strain relaxed buffer layers was typically a few $10^7\,\mathrm{cm}^{-2}$. Prior to GaAs epitaxy, we have performed an ozone-based wet cleaning of the Ge surface in order to remove contaminants, particles, and the native oxide. A Siconi$^{\mathrm{TM}}$ surface treatment[14] was performed in the MOVPE tool before growth in order to remove any remaining oxides from the Ge surface. Once loaded in the MOVPE chamber, a hydrogen bake was performed at 20 Torr and at a temperature higher than 700 °C followed by growth of 300 nm GaAs between 500 °C and 700 °C and at a pressure between 20 and 100 Torr. The growth conditions for all three layers were identical apart from the different substrates used. We have used atomic force microscopy to probe the surface roughness and measure the APB density in those GaAs layers. High resolution X-ray diffraction measurements were performed to evaluate the GaAs crystallinity.

High resolution X-ray diffraction omega-2theta scans of the (004) peak are plotted in Figure 1 for GaAs layers grown on 0.1°, 0.3°, and 0.5° offcut substrates, with each scan showing three peaks. The inset shows a magnification of the XRD peaks of the Ge and GaAs layers. The most intense peak at a 34.56° originates from the silicon substrate. Next, just above 33°, the peak corresponds to the germanium strain relaxed buffer. Finally, the third peak at around 33.1° corresponds to the GaAs layer. The thick GaAs and Ge layers are single crystals: diffraction peaks are intense and sharp. From the angular position of the XRD peaks, we can deduce the degree of strain relaxation R of the Ge and GaAs layers. We obtained a macroscopic degree of strain relaxation R of 104% for the Ge strain relaxed buffer regardless of the offcut of the silicon substrate, showing that the Ge layer is under tensile strain in agreement with Ref. 13 because of the difference in the thermal expansion coefficient between silicon and the germanium. The degree of strain relaxation of the GaAs layer is 106%, regardless of the offcut of the silicon substrate, meaning that the GaAs layer is also under tensile strain. This is an expected behavior for thin films with larger coefficients of thermal expansion than the substrates they are grown on. The Full Width at Half Maximum (FWHM) of the GaAs layers' peak is slightly larger for a substrate offcut of 0.1° (0.019°) than for a substrate offcut of 0.3 and 0.5° (0.013° and 0.014°, respectively). This likely means that the crystalline quality is higher for larger offcuts.



Sample	Miscut (°)	APB density (µm^{-1})
a	0.1	2.8
b	0.3	0.3
c	0.5	0

FIG. 2. $5 \times 5\ \mu\mathrm{m}^2$ AFM images of the surface of GaAs layers grown on Ge-buffered silicon(001) substrates with three different offcut angles: (a) 0.1° offcut angle, (b) 0.3° offcut angle, and (c) 0.5° offcut angle. All the offcut angles are in the ⟨110⟩ direction. The scale on the right hand side of each image is labeled in nm. The table (d) presents the APB density measured for each sample. AFM image sides are along the ⟨100⟩ directions.

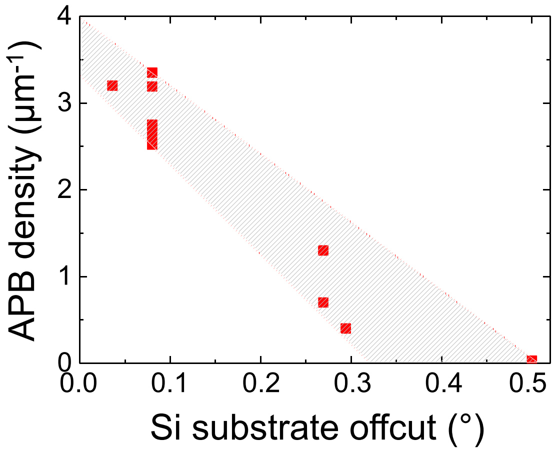


FIG. 3. Plot of the APB density versus the offcut angle of the silicon substrate used for Ge then GaAs growth.

Figure 2 shows 5×5 μm^2 AFM images of the surface morphology of the GaAs epilayers. Images (a), (b), and (c) correspond to GaAs layers on silicon substrates with offcuts of 0.1°, 0.3°, and 0.5°, respectively, with APBs appearing as darker lines on those images. The APB density was obtained by (i) measuring the total APB length in a given area, and (ii) dividing the resulting length by the area. It is therefore expressed in $\mu m/\mu m^2$, i.e., in μm^{-1}. The density is 2.8 μm^{-1} for the GaAs grown on a 0.1° offcut silicon substrate, but only 0.3 μm^{-1} on a 0.3° offcut substrate. On a 0.5° offcut substrate, we have a single domain GaAs layer with no APBs.

Figure 3 is a plot of the APB density measured for several samples grown on offcut substrates with different offcut angles, always in the $\langle 110 \rangle$ crystalline direction. For growth performed on substrates with an offcut of 0.1° or less, the antiphase boundary density is between 2.5 and 3.5 μm^{-1}, despite slight growth variations between samples. The three GaAs layers grown on substrates with a 0.3° offcut angle have an APB density between 0.3 and 1.4 μm^{-1}. Finally, on 0.5° offcut silicon substrates, we obtain single domain GaAs epilayers even for slight variations in the epitaxial growth sequence.

Finally, in Figure 4, we have imaged the surface topology of the Ge strain relaxed buffer (the surface on which GaAs growth starts) for two different silicon offcut angles: 0.04° (left) and 0.3° (right). As expected, the offcut angle of the starting silicon substrate influences the density of terraces. Note that the size of the two images is not the same: it was chosen in order to display a similar number of terraces. In addition, we can see that the left image does not show any clear direction for the steps; they are randomly oriented. This is due to the fact that for such low offcut angle, it is hard for the substrate manufacturer to produce the offcut in a specific crystalline direction. The right image exhibits parallel steps perpendicular to the [110] direction, as expected due to the intentional offcut. On the left image, there are 11 terraces over 5 μm; the average terrace length is around 450 nm. According to X-Ray diffraction measurements, the offcut of the substrate was 0.04°, which would give a bi-atomic step spacing of 405 nm, showing that the results are coherent. On the right hand image, there are 36 terraces over 2.8 μm, translating into an average terrace length of 78 nm. The offcut of this substrate as measured by X-Ray diffraction was 0.28°, which should give a terrace length of 58 nm for bi-atomic steps. Once again, the two measurements are coherent.

Besides APBs, the other main crystalline defect of concern in GaAs epitaxial films on silicon is threading dislocations. The threading dislocation density in the GaAs films is expected to be close to that in the germanium strain relaxed buffer underneath (i.e., a few $10^7\,cm^{-2}$). Preliminary cathodo-luminescence results yielded a threading dislocation density between 5×10^7 and $10^8\,cm^{-2}$ as expected (with a limited field of view, however, that might hamper accuracy since the distribution of threading dislocations is not uniform). This value is also similar to the model proposed by Wang *et al.*[15] that predicts a threading dislocation density between 1×10^7 and $5 \times 10^7\,cm^{-2}$ for the total deposited thickness that we obtained.

Using offcut substrates has for a long time been considered essential when growing polar materials (e.g., GaAs) on (001) orientated non-polar substrates (e.g., silicon), in order to avoid the presence of APBs in epilayers. Most research groups have used (001) substrates with a 4° to 6° offcut in the $\langle 110 \rangle$ direction. The influence of small offcut angles (e.g., 0.5° and less) on the properties of GaAs grown on Ge-buffered silicon (001) substrates has been less studied. There will always be small offcut angle variations on nominally

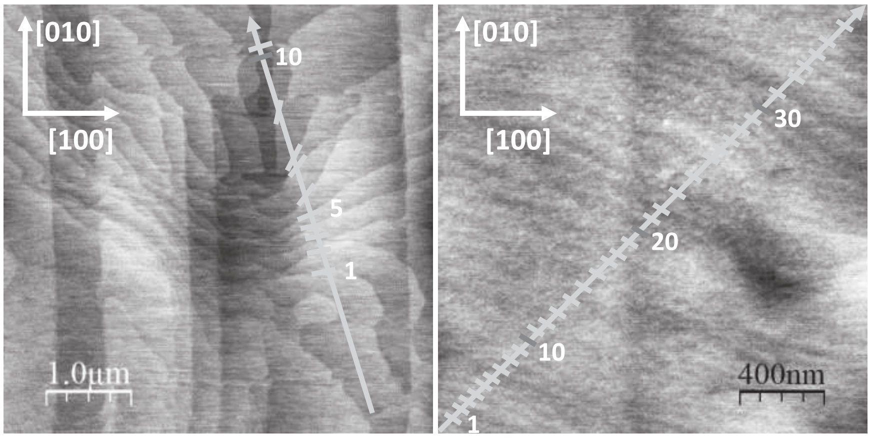


FIG. 4. Atomic Force Microscopy images of the Ge surface of samples grown on two different offcut angle silicon substrates. The left image corresponds to a 0.04° offcut (001) substrate, and the right image corresponds to a 0.28° offcut (001) substrate.

on-axis substrates, and a close examination of the resulting properties as a function of the offcut angle is shown in Figure 3. We have found that small offcut variations greatly influence how GaAs grows on Ge-buffered silicon substrates and that the offcut angle that yields single domain layers in MOVPE can be as low as 0.5° instead of the 4°–6° angle typically found in the literature. A previous report for the growth of GaP on nearly lattice-matched silicon substrates, prepared by hydrogen bakes at temperatures higher than 950 °C and silicon buffer layer, highlighted the effect of 0.1°–0.2° offcut from nominally exact (001) oriented silicon.[16] We show that further slight offcut from nominal along with intermediate Ge layer eliminates the requirement for such high temperature silicon preparation and enables blanket APB-free GaAs epifilms on lattice-mismatched silicon.

We explain the mechanism to eliminate the antiphase domains as follows: AFM images in Fig. 4, in addition to the known offcut of the substrate, clearly show that we have bi-atomic steps between two adjacent terraces. But it seems that having bi-atomic high steps is not enough to achieve the epitaxy of a single domain GaAs layer, because in that case, we should obtain single GaAs domain on Ge surfaces whatever the offcut of the Ge surface. This is not what we have observed. More surprisingly, antiphase domains have also been observed on high offcut angle Ge substrates. Hudait *et al*. have observed antiphase domains on 6° offcut substrates.[17] We can therefore suggest that bi-atomic steps are a necessary but not a sufficient condition to avoid anti-phase boundaries because (i) the arsenic coverage might not be 100% efficient on the Ge surface or (ii) there could remain some single atomic steps on the Ge surface or (iii) step edges can be rough[18] or (iv) arsenic exposure might modify the surface reconstruction.[19] In addition to having bi-atomic steps, it seems that the primary criterion is the distance between steps. In our case and with identical growth conditions, we could achieve single domain GaAs films only on substrates with an offcut of 0.5°, i.e., with a mean spacing between steps of 32 nm, and not if the mean spacing was 58 nm. It is likely that we cannot avoid anti-phase boundaries appearing in the early stages of growth, but if they are close enough together and growth conditions are adequate, they will all annihilate. Indeed, they tend to propagate on {011} planes[20] and therefore annihilate when the film gets thicker. Therefore, achieving APB-free GaAs epitaxial films on Ge requires several conditions: being below a threshold value for the distance between the atomic steps, and using the correct growth conditions to annihilate the APBs.

We have grown 300 nm thick GaAs epilayers by MOVPE on one micron thick Ge strain relaxed buffers, themselves grown on silicon (001) substrates. XRD analysis shows that we have obtained high quality GaAs layers that were slightly tensile strained ($R = 106\%$), and AFM shows that the GaAs layers were smooth (1.3 nm RMS roughness for $5 \times 5\ \mu m^2$ images). We have performed the growth on "quasi-nominal" (001) silicon substrates with an offcut of up to 0.5° finding that small offcut angles can greatly influence the density of antiphase boundaries of the GaAs epilayer. We reproducibly obtained APB-free GaAs epilayers on (001) silicon substrates with a very small offcut angle: 0.5° in the $\langle 110 \rangle$ direction. We propose that the distance between adjacent atomic steps is critical for achieving APB-free GaAs epitaxial films on Ge strain relaxed buffers grown on silicon substrates.

This work has been partially supported by the LabEx Minos ANR-10-LABX-55-01 and the French "Recherches Technologiques de Base" and RENATECH programs. The authors would sincerely like to thank Stephane Puget from AMAT for technical assistance on the MOVPE tool and Jérôme Siviniant from Sun Edison for fruitful scientific discussions on silicon substrates.

[1] V. K. Yang, M. Groenert, C. W. Leitz, A. J. Pitera, M. T. Currie, and E. A. Fitzgerald, J. Appl. Phys. **93**(7), 3859 (2003).
[2] D. Colombo, E. Grilli, M. Guzzi, S. Sanguinetti, S. Marchionna, M. Bonfanti, A. Fedorov, H. von Känel, G. Isella, and E. Müller, J. Appl. Phys. **101**, 103519 (2007).
[3] S. F. Fang, K. Adomi, S. Lyer, H. Morkoç, H. Zabel, C. Choi, and N. Otsuka, J. Appl. Phys. **68**(7), R31 (1990).
[4] Y. Chriqui, L. Largeau, G. Patriarche, G. Saint-Girons, S. Bouchoule, I. Sagnes, D. Bensahel, Y. Campidelli, and O. Kermarrec, J. Cryst. Growth **265**, 53 (2004).
[5] Y. B. Bolkhovityanov and O. P. Pchelyakov, Phys. –Usp. **51**(5), 437 (2008).
[6] M. Kawabe and T. Ueda, Jpn. J. Appl. Phys., Part 2 **25**(4), L285 (1986).
[7] S. K. Agarwal, R. Tyagi, M. Singh, and R. K. Jain, Sol. Energy Mater. Sol. Cells **59**, 19 (1999).
[8] S. M. Ting and E. A. Fitzgerald, J. Appl. Phys. **87**(5), 2618 (2000).
[9] J. A. Carlin, S. A. Ringel, E. A. Fitzgerald, and M. Bulsara, Sol. Energy Mater. Sol. Cells **66**, 621 (2001).
[10] D. Choi, J. S. Harris, E. Kim, P. C. McIntyre, J. Cagnon, and S. Stemmer, J. Cryst. Growth **311**, 1962 (2009).
[11] W. Hu, B. Cheng, C. Xue, S. Su, Z. Liu, Y. Li, Q. Wang, L. Wang, J. Liu, J. Ding, G. Lin, and Z. Lin, Thin Solid Films **520**, 5361 (2012).
[12] Q. Li, K. W. Ng, and K. M. Lau, Appl. Phys. Lett. **106**, 072105 (2015).
[13] J. M. Hartmann, A. Abbadie, N. Cherkashin, H. Grampeix, and L. Clavelier, Semicond. Sci. Technol. **24**, 055002 (2009).
[14] R. Yang, N. Su, P. Bonfanti, J. Nie, J. Ning, and T. T. Li, J. Vac. Sci. Technol. B **28**, 56 (2010).
[15] G. Wang, R. Loo, E. Simoen, L. Souriau, M. Caymax, M. M. Heyns, and B. Blanpain, Appl. Phys. Lett. **94**, 102115 (2009).
[16] I. Németh, B. Kunert, W. Stolz, and K. Volz, J. Cryst. Growth **310**, 1595 (2008).
[17] M. K. Hudait and S. B. Krupanidhi, J. Appl. Phys. **89**(11), 5972 (2001).
[18] B. A. G. Kersten, H. J. W. Zandvliet, D. H. A. Blank, and A. V. Silfhout, Surf. Sci. **322**, 1 (1995).
[19] S. Gan, L. Li, M. J. Begarney, D. Law, B.-K. Han, and R. F. Hicks, J. Appl. Phys. **85**(3), 2004 (1999).
[20] Y. Li and L. J. Gilling, J. Cryst. Growth **163**, 203 (1996).