Confined selective lateral epitaxial growth of 16-nm thick Ge nanostructures on SOI substrates: Advantages and challenges

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In this contribution, we report on the growth of Ge inside extremely thin 16-nm thick cavities through selective lateral growth of Ge on 300 mm silicon-on-insulator (0 0 1) substrates. We showed that the density of defects depends on the cavity shape, with extended defects such as micro-twins and stacking faults observed on the top surface along the ⟨1 1 0⟩ directions when the Si/Ge growth interface is along the ⟨1 1 0⟩ directions. The optimization of the cavity shape, by tuning the etching conditions, leads to a significant reduction of the defects in the Ge nanostructures, and this approach paves the road towards the co-integration of Si and Ge based devices.

1. Introduction

To date, silicon is by far the most used material in the semiconductor industry for several reasons, namely its high purity, low cost, large area of the substrates, mature technology and the stability of its oxide. However, the increasing demand for enhanced opto-electrical device performance necessitates the integration of new materials with superior physical properties. Thus, significant efforts have been made to integrate materials such as III-V, SiC and Ge on Si substrates [1–4]. Among those materials, Ge represents a very interesting compromise between the challenges that have to be resolved and the advantages that this material offers. Ge has a diamond crystal structure similar to that of Si, which prevents the formation of antiphase boundaries, conventionally observed during the growth of polar semiconductors on Si substrates [5,6]. In addition, the lattice mismatch between Ge and Si is 4.2%, far below that between InAs or SiC and Si. Ge possesses a hole mobility four times higher than Si, making it a suitable candidate for p-type metal-oxide-semiconductor transistors, and it can be used for photodetectors operating in the low loss windows of waveguides, due to its band gap of 0.8 eV at room temperature [7,8]. Finally, by submitting Ge to tensile strain, it can be turned into a direct band gap material [9].

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The growth of Ge on Si substrates is well documented in literature, with several approaches explored to obtain high crystal quality [3,10–15]. In this article, we will focus on the confined selective lateral growth of Ge on silicon-on-insulator (SOI) substrates which offers the possibility of integrating Si and Ge based devices with the same overall process flow. Yamamoto et al. have reported on the local integration of 300 nm thick Ge on SOI substrates through confined lateral growth [16]. They have observed the presence of dislocations which ran along the ⟨1 1 0⟩ directions, while defect-free Ge was obtained along the ⟨0 1 0⟩ directions. Lateral growth allows the removal of any defective parts by etching, unlike the vertical approaches, such as aspect ratio trapping. Furthermore, smooth Ge layers can be obtained using this method, avoiding thereby the necessity of an additional chemical mechanical polishing step. Finally, with this approach, Ge and Si will be at the same height of the substrate surface, which markedly simplifies the co-integration of devices using these two materials.

In this contribution, we report on the confined lateral growth of Ge inside 16-nm-thick cavities. The cavities are formed by etching a silicon layer stacked between two oxide layers, through circular openings. In a first part, we will discuss the influence of temperature on the growth of Ge nanostructures. Structural and morphological inspections are performed to understand the nature of defects in these nanostructures. Afterwards, based on our observations, we suggest modifications to the cavity shape in order to significantly reduce the density of defects in the grown Ge nanostructures.

2. Experimental details

For this study, we used 300 mm on-axis silicon-on-insulator (0 0 1) substrates with 16 nm thick Si layers on top of 145 nm thick buried oxide (BOX). Low-pressure chemical vapor deposition (LP-CVD) was used to deposit a 70 nm thick oxide on top of the SOI substrate to subsequently confine the growth in the lateral directions. Afterwards, holes were dry etched into the top oxide layer in order to create a path to the Si layer. An HF-last wet cleaning was performed prior to the introduction of the wafers in the ASM Epsilon 3200 reduced pressure CVD chamber. An HCl vapor phase etching in hydrogen was performed to laterally etch the Si and create cavities between the two oxides, as known in literature [16–18]. The pressure was set at 80 Torr during this step, while the F(HCl)/F(H_2) mass-flow ratio was equal to 0.0188. Finally, Ge was selectively grown inside those cavities using germane (GeH_4) diluted at 10% in H_2. The temperature varied from 400 °C to 550 °C. At 400 °C, a pressure of 80 Torr was used with F(GeH_4)/F(H_2) = 0.001, while for 500 °C and 550 °C, the pressure was 20 Torr and the F(GeH_4)/F(H_2) ratio was 0.0006. Fig. 1 shows the process used to create hollow cavities subsequently filled with Ge.

The Ge nanostructures were characterized by scanning electron microscopy (SEM) in a Zeiss Merlin, with atomic force microscopy (AFM) and scanning spreading resistance microscopy (SSRM) performed on a Bruker Dimension Icon tool. We used a p-doped diamond coated silicon tip (CDT-NCHR from Nanosensors) with a nominal spring constant of 40 N/m for the scanning probe measurements which were performed in a nitrogen-filled glove box (MBraun) with H_2O and O_2 content below 3 ppm. For transmission electron microscopy (TEM) sample preparation, focused ion beam (FIB) was used to cut out a lamella at the desired area. All TEM images were acquired in a Tecnai FEI microscope operating at 200 kV, or in a Jeol 3010 microscope operating at 300 kV.

3. Results

3.1. Growth conditions and structural investigations

As described above, cavities were etched into a silicon layer sandwiched between two oxide layers. The Si etch rate along the ⟨1 1 0⟩ directions is 260 nm min^{-1}, and 240 nm min^{-1} along the ⟨0 1 0⟩ directions, leading to an octagonal cavity shape due to the almost isotropic in-plane etching conditions (cf. Fig. 1). Fig. 2 shows plan-view SEM images of the Ge nanostructures grown at different temperatures inside these cavities. The Ge homogenously fills the cavities for all three growth temperatures. Above this temperature, the growth turns into 3D and voids are observed when different crystals coalesce (not shown here). The growth is initiated at 400 °C for all 3 samples, because if the growth is initiated directly at higher temperatures (above 500 °C), 3D island growth is observed. This tendency is similar to the growth of Ge on blanket Si substrates [3,10]. For the growth at 400 °C and 80 Torr, the growth rate is 10 nm min^{-1}. Similar growth rate is obtained when the growth is performed at 500 °C and 20 Torr. The increase of the growth rate that should be observed with increasing temperature is compensated by the reduction of pressure which typically reduces the growth rate. For the nanostructures grown at 550 °C and 20 Torr, the growth rate is 14 nm min^{-1}.

The oxide cap was removed by an HF wet etching step and the Si and Ge imaged with SEM and scanning probe microscopy. The SEM image (Fig. 3a) shows a dark contrast in the Ge nanostructures along the ⟨1 1 0⟩ crystallographic directions which was observed in all cases regardless of the growth conditions. The AFM image (Fig. 3b) showed an abrupt interface between Si and Ge, and the surface morphology of the Ge nanostructures was homogenous without any additional contrast of the defects in the ⟨1 1 0⟩ directions seen by SEM. This is also the case for the SSRM measurements as shown in Fig. 3c, showing that the Ge is electrically homogenous regardless of the crystallographic directions and the Ge resistivity is lower than that of Si as expected.

Fig. 4 shows a cross sectional TEM image of a Ge nanostructure, sandwiched between two oxide layers, along the [1 1 0] zone axis. The high resolution TEM image (Fig. 4b) shows that there is extensive twinning on inclined {1 1 1} planes which occur along the ⟨1 1 0⟩ growth directions. The Fast Fourier Transform (FFT) shown as inset reveals the presence of additional diffraction spots, indicated by white circles. These spots demonstrate the presence of microtwins in addition to stacking faults in the Ge nanostructures. There are no surface irregularities caused by those defects, most likely because of the presence of the cap oxide, which explains the

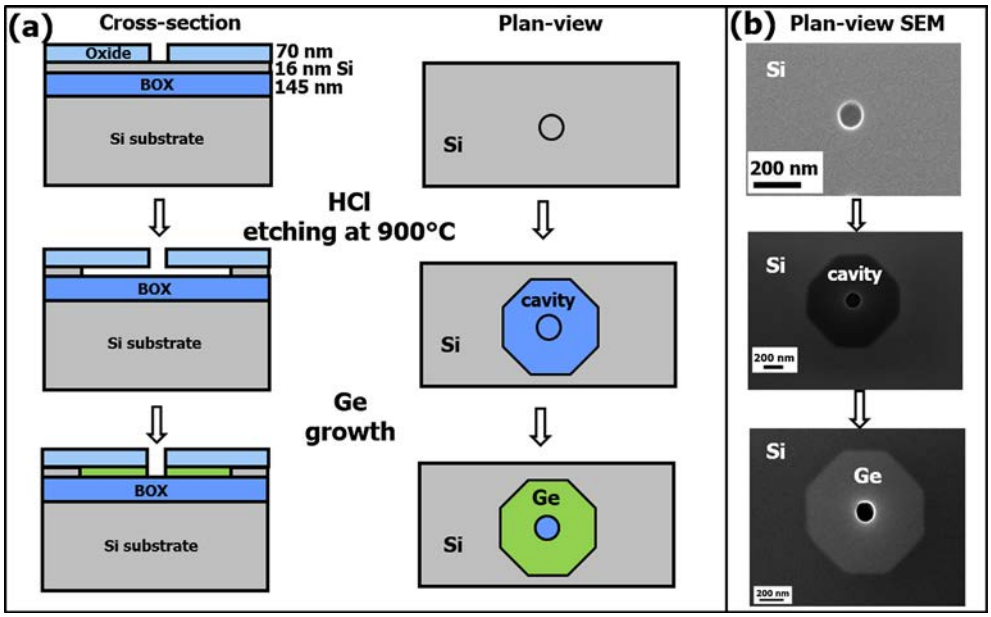

Fig. 1. (a) Schematic depiction of the process flow used to integrate Ge on SOI substrates. The top oxide is not represented in the plane-view drawings for clarity. (b) Corresponding plane-view SEM images (the oxide cap layer is transparent for the electrons).

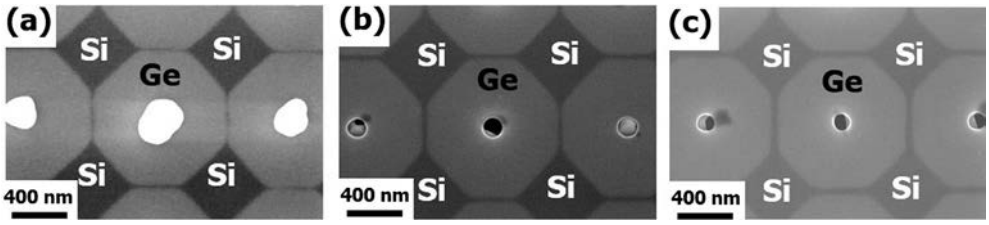

Fig. 2. Plan-view SEM image of the Ge nanostructures grown at (a) 400 °C, (b) 400 °C nucleation then growth at 500 °C and (c) 400 °C nucleation then growth at 550 °C.

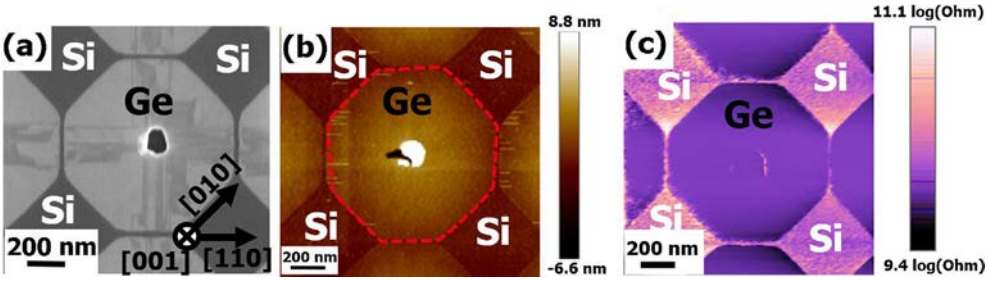

Fig. 3. (a) Plan-view SEM image after oxide cap removal, (b) corresponding AFM image and (c) corresponding SSRM image (Bias sample −1 V).

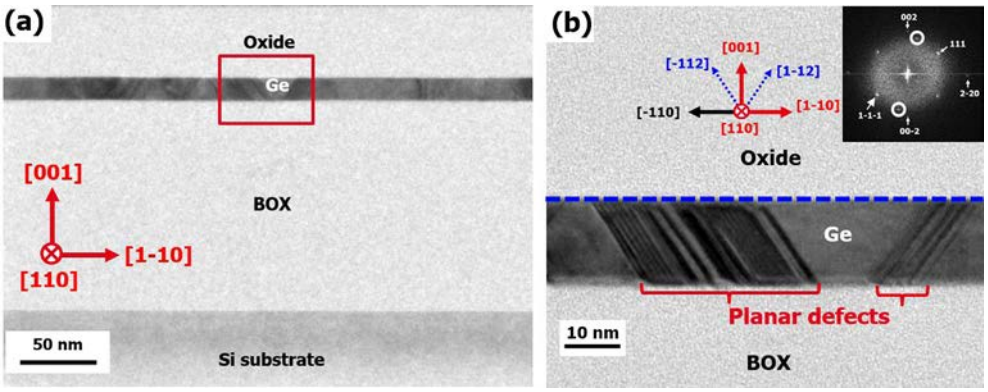

Fig. 4. (a) Cross-sectional TEM image of the Ge nanostructure sandwiched between two oxide layers. (b) High resolution TEM image of the area indicated by the red rectangle, showing the presence of defects on the {1 1 1} planes of the Ge nanostructure. The inset represents the corresponding FFT. The additional diffraction spots, originating from micro-twins, are indicated by white circles.

smooth Ge surface observed in the AFM image after cap oxide removal.

3.2. Optimizing the cavity shape

Following the SEM and TEM observations which highlighted the presence of defects in the Ge nanostructures, in particular when the Si/Ge growth interface is directed along the ⟨1 1 0⟩ directions, the cavity shape was tuned to reduce the defect density by avoiding these ⟨1 1 0⟩ oriented interfaces. This required the optimization of the etching process to favor the anisotropic etching of Si. It has been shown that the temperature plays a crucial role in determining the HCl etching regime of Si [17], and so we reduced the etching temperature from 900 °C to 800 °C and increased the HCl flux (to retain a reasonable etch rate). The F(HCl)/F(H_2) mass-flow ratio was 0.75 in this case. With these process conditions, the etching rate was highly anisotropic, with 27 nm min^{-1} along the ⟨1 1 0⟩ directions and 16 nm min^{-1} along the ⟨0 1 0⟩ directions. This led to square cavity formation with ⟨0 1 0⟩ sidewalls, as shown in Fig. 5a. Fig. 5b shows the Ge surface after oxide cap removal, with the red arrows indicating the defective areas in the Ge nanostructure which are once again along the ⟨1 1 0⟩ directions. The density of defects is significantly reduced compared to Ge grown inside octagonal cavities.

Fig. 6 shows HR-TEM images of the Ge nanostructures along the [1 1 0] zone axis. The interface between Si and Ge is abrupt, with a well-defined {1 1 0} vertical facet, and micro-twins and stacking

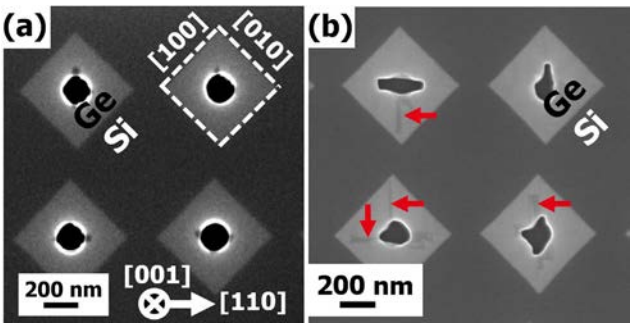

Fig. 5. Plan-view SEM images of the Ge nanostructures with square shaped ⟨1 0 0⟩ cavities (a) prior to oxide cap removal and (b) after oxide cap removal. The red arrows indicate the dark contrast in the Ge nanostructures.

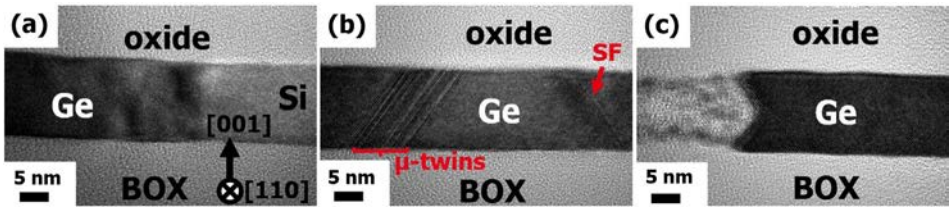

Fig. 6. HR-TEM images of the (a) Si/Ge interface, (b) defects in the Ge nanostructure and (c) free-edge of the Ge nanostructure. The images were acquired along the [1 1 0] direction.

faults are observed along the {1 1 1} planes. However, the width of the defective Ge area is significantly reduced compared to that in octagonal cavities. We can conclude that the defects have a major dependence on the cavity shape, and that although their complete elimination appears to be a difficult task, their propagation area can be minimized by controlling the cavity shape. Nevertheless, such defects do not dramatically impact the electrical properties of the material [19].

4. Conclusion

In this contribution, we demonstrated the possibility of locally integrating Ge on insulator in extremely confined cavities (16 nm thick). We showed that, in the case of octagonal cavities, a high density of micro-twins was observed, on the top surface, along the ⟨1 1 0⟩ directions when the growth was initiated from ⟨1 1 0⟩ oriented growth interface. By tuning the etching conditions, we succeeded in eliminating the growth interfaces along these directions, leading to a significant reduction of the micro-twins density. Nevertheless, some micro-twins are still observed along the ⟨1 1 0⟩ directions in square cavities. This integration scheme can be advantageous for the fabrication of Si and Ge based devices electrically isolated from the substrates by the buried oxide layer.

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