Improvement of Sidewall Roughness of Sub-Micron SOI Waveguides by Hydrogen Plasma and Annealing

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***Abstract*— We report the successful fabrication of low-loss submicrometric silicon-on-insulator strip waveguides for on-chip links. Postlithography treatment and postetching hydrogen annealing have been used to smoothen the waveguide sidewalls, as roughness is the major source of transmission losses. An extremely low silicon line-edge roughness of 0.75 nm is obtained with the optimized process flow. As a result, record-low optical losses of less than 0.5 dB/cm are measured at 1310 nm for strip waveguide dimensions exceeding 500 nm. They range from 1.2 to 0.8 dB/cm for 300–400-nm-wide waveguides. Those results are to our knowledge the best ever published for a 1310-nm wavelength. These results are compared to modeling based on Payne and Lacey equations.**

***Index Terms*— Silicon waveguide patterning, line edge roughness (LER), smoothing treatments, optical losses, photonic integrated circuits (PICs).**

I. Introduction

THE silicon–on-insulator (SOI) optical circuitry is a critical building block for the realization of a large variety of on-chip photonic components [1]. The Si transparency at optical communications wavelengths and the high refractive index contrast between Si and SiO_2 result in an efficient light confinement in the silicon guiding layer. Optical chips can thus be miniaturized. The main drawback of extreme light confinement in small-cross-section Si waveguides is the high sensitivity of light to SiO_2/Si interface imperfections resulting from the fabrication process [2]. In particular, the waveguide sidewalls roughness, or line-edge roughness (LER), has a direct impact on propagation losses by light scattering. This becomes increasingly problematic with the waveguide dimensions decrease since it enhances interactions between light and rough sidewalls [3]. Losses by light scattering at the core/cladding interface are usually predominant in sub-micron undoped silicon waveguides compared to other sources of losses that can be due to either absorption by defects or leakage towards the substrate, or non-linear effects or even the lack of field confinement [4]. Several approaches have been proposed to smooth the silicon pattern sidewalls either by optimizing the waveguide patterning [5] or by adding post-processing methods [6] such as thermal annealing under H_2 [7].

Nowadays, propagation losses < 2 dB/cm for silicon strip waveguides with 500 nm $\times$ 220 nm cross-section are commonly obtained [5], [8]. However, achieving really low loss values below 1 dB/cm remains challenging, although some research groups have already reported such record values [5], [9], [10].

In this article, we propose post-lithography and post-silicon etching treatments to fabricate sub-micron undoped silicon waveguides in SOI wafers with minimal sidewall surface roughness and minimal critical dimension (CD) loss, in order to decrease the propagation losses below 1 dB/cm at telecom wavelengths (both 1310 nm and 1550 nm). This article shows that a record-low silicon LER of 0.75 nm is obtained by using H_2 plasma post-lithography treatment and H_2 thermal annealing after silicon etching. As a result, record optical losses less than 1 dB/cm have been obtained for CDs larger than 390 nm, and ranged between 1.2-0.8 dB/cm for 300-400 nm wide waveguides. Propagation losses are also compared to a model based on Payne and Lacey equations taking into account scattering losses only [3].

II. Experimental Setup

A. Substrates

Si/SiO_2 strip waveguides are fabricated on 200-mm diameter SOI wafers with 310-nm-thick crystalline undoped silicon layers on top of 800-nm-thick SiO_2 buried oxides (BOX), using a classical top-down approach. Wafers are patterned with 193-nm lithography in an ASML1100 stepper. A lithographic mask has been designed with lines having CDs ranging from 200 nm to 800 nm. The lithography stack coated on the SOI wafers comprises a 400-nm-thick 193 nm photoresist (PR) layer on top of a 82-nm-thick bottom antireflective coating (BARC) layer.

B. Plasma Etching Tool and Processes

Etching experiments are performed in a high-density plasma reactor generating an inductively coupled plasma (ICP). The waveguide patterning baseline process (BP) flow is the following: a HBr plasma treatment is used to cure the PR

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prior to etching [9]. Then, the BARC is opened with an $Ar/Cl_2/O_2$ plasma and the silicon waveguides are etched using an $HBr/Cl_2/He\text{-}O_2$ plasma. Finally the resist/BARC layers are stripped under O_2 plasma. Once the waveguides are patterned, a 100-nm SiO_2 hard mask was deposited and the wafers exposed to a second lithography step dedicated to the patterning of fiber grating couplers. After the etching of couplers, a 1.1-μm-thick SiO_2 layer is deposited on the wafer to encapsulate the silicon waveguides. More details on the process flow can be found in [10].

C. Smoothing Techniques

Post-lithography treatments can be used to smooth photoresist patterns prior to plasma etching transfer and thus to improve the final LER [11]. In [13], we reported that H_2 plasma treatment was the most efficient to decrease the PR LER and is used in this work. H_2 thermal annealing at 850 °C during 2 min is also applied to smooth the Si sidewalls after etching. The hydrogen flow was several tens of standard liters per minute and the epitaxy chamber pressure was 20 Torr.

D. Process Characterization

After silicon waveguide patterning, waveguide profiles were imaged by scanning electron microscopy (SEM). The CD and LER of the patterns are determined from top-view images taken by Hitachi CG4000 CD-SEM. The LER metrology is performed on the 400-nm-wide patterns only. Spectral analyses of the roughness are performed using the power spectral density (PSD) fitting method proposed by Azarnouche *et al.* [13]. This method allows the extraction of unbiased LER values (roughness amplitude at 3σ) and correlation length L_c. More details on the method can be found in [12] and [13].

E. Optical Measurements

An on-wafer fiber probe system is used to characterize the propagation loss of the waveguides. A laser beam is coupled into and out of the structured waveguides via Transverse Electric-polarized grating couplers. A wavelength scan is performed in the 1260-1360 nm wavelength range and in the 1500-1600 nm wavelength range to compute losses at 1310 nm and at 1550 nm. The power used is 1mW at 1310 nm and 5 mW at 1550 nm, such that losses due to nonlinear effects are negligible. The transmitted power of the laser light through the waveguide is measured by a spectrum analyzer connected to the output fiber. Seven measurements are performed on waveguides with different lengths ranging from 2.2 mm up to 198 mm. When bends are necessary, the radius of curvature is 30 μm such that bending losses are negligible at non-critical confinement factors. This set of measurements is repeated for seven waveguide's widths (ranging from 200 nm to 800 nm) on three dies of the wafer. The propagation loss reported in this work is the average of the measurements performed on each of the three dies over the wafer. Accuracy of the probe system is $\pm$ 0.05 dB/cm.

F. Simulations Work

Scattering losses are simulated using the model proposed by Payne and Lacey [3], developed for planar waveguides. This two-dimensional (2D) analytical scattering-loss model takes into account the waveguide geometry (height and width) and roughness parameters (LER and the correlation length L_c). The scattering losses α, in dB/cm, are given by the following equation:

$$\alpha = \frac{\sigma^2}{\sqrt{2}k_0 d^4 n_1} g f_e \qquad (1)$$

where σ is the Root Mean Square (RMS) roughness of the guide sidewalls (LER $= 3\sigma$), $k_0 = 2\pi/\lambda$ is the free-space wavenumber, λ the wavelength (λ = 1310nm or 1550 nm in this study), d the half-width of the waveguide (ranging from 100 to 400 nm), n_1 the Si core index ($n_1 = 3.5$), g a function that depends on k_0, d, n_1 and n_2 the SiO_2 cladding index ($n_2 = 1.44$). The function f_e depends on the correlation length L_c, k_0, d, n_1, n_2, and n_{eff} the effective index of the waveguide. In our study, the effective index was computed via a finite-element method (FEM) software for each of the waveguide dimensions and wavelengths. The roughness parameters introduced in the model are those obtained experimentally by the PSD fitting method. Nevertheless, this model does not take into account sources of optical losses other than scattering losses.

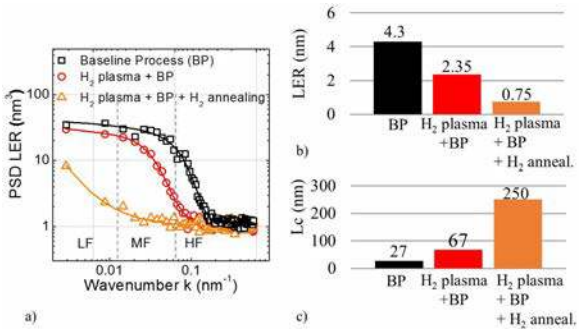

Fig. 1. Roughness characterization using the Power Spectral Density (PSD) fitting method of silicon waveguides patterned with and without smoothening treatments. Two treatments are investigated: post-lithography H_2 plasma treatment and post-etching H_2 thermal annealing: a) PSD graphs for Line-Edge Roughness (PSD LER). HF, MF and LF correspond to high-frequency, medium-frequency and low-frequency regions, respectively; b) LER c) correlation length (L_c).

III. Experimental Results

A. Effects of Pre- and Post-Etching Treatments on the Silicon Waveguide Roughness

Fig. 1 compares the roughness spectral distribution [Fig. 1(a)], the roughness amplitude (LER) [cf. Fig. 1(b)], and the correlation length (L_c) [Fig.1(c)] after silicon patterning with and without smoothening treatments. Two treatments are investigated: post-lithography H_2 plasma treatment and post-etching H_2 thermal annealing. First, it is observed that the introduction of H_2 plasma treatment prior to etching allowed a decrease of the silicon LER of about 45% compared to the BP (from 4.3 nm down to 2.35 nm, [Fig. 1(b)]). This decrease is also accompanied by a correlation length increase [Fig. 1(c)]. This trend is reflected on the PSD graph by a decrease of the high- and medium–frequency roughness components. The H_2 plasma smoothening effect has been explained elsewhere [11], [12]. Briefly, the wavelengths below 200 nm emitted by H_2 plasma chemically modifies the photoresist bulk, resulting in resist flowing and surface smoothening. The smoothed resist sidewalls roughness is then transferred into the silicon waveguide during plasma patterning.

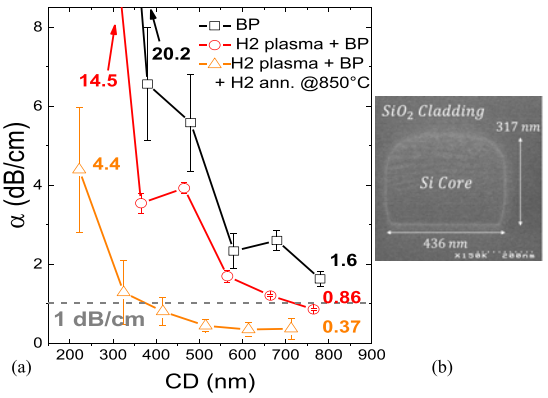

Fig. 2. (a) Experimental optical losses measured at 1310 nm for waveguides patterned with and without smoothening treatments as a function of the waveguide's width. (b) Cross-sectional SEM image of the Si waveguide patterned with H_2 plasma treatment and H_2 annealing after encapsulation with the SiO_2 cladding.

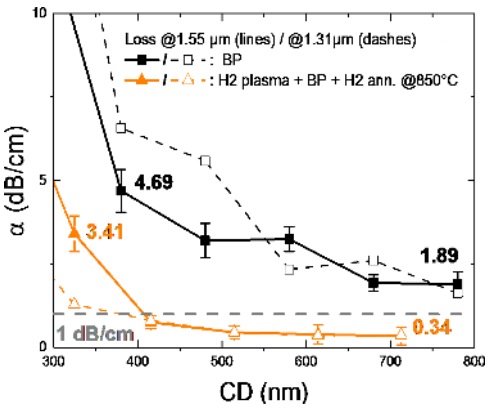

Fig. 3. Comparison between experimental optical losses measured at 1310 nm (full lines) and 1550 nm (dashed lines) for the baseline process and the optimized process.

The impact of H_2 thermal annealing on the silicon waveguide roughness is also reported in Fig. 1. H_2 thermal annealing allows to decrease the LER by 68% compared to the BP, resulting in an extremely low LER value of 0.75. It is also clear in Fig. 1(a) that H_2 annealing significantly reduces all frequency components, even the low-frequency ones that are usually hard to eliminate by conventional smoothening methods [12]. The PSD fitting method provides a correlation length of 250 nm after H_2 annealing. However, the accuracy of this estimation is questionable. Indeed, a correlation length can properly be extracted from PSD fitting if the PSD presents a plateau in the low-frequencies region, which is not the case after H_2 annealing. Anyway, it can be concluded that L_c is drastically increased after H_2 thermal annealing and is higher than 150 nm according to PSD analysis. After H_2 thermal annealing, the shape of the waveguide remained relatively square except at the four corners that have been slightly rounded [cf. Fig. 2(b)], such that optical modes are not significantly affected. Moreover the waveguide width loss is only of 30 nm compared to the BP, making this treatment compatible with the whole integration.

Some other work already reported similar silicon sidewalls roughness reduction after H_2 thermal annealing using other process conditions, and generally for applications other than waveguide patterning [14], [15]. Si smoothening by H_2 annealing is based on the theory of surface atomic migration. When heating silicon in H_2 at temperatures lower than its melting point (1414 °C), silicon atoms on free surfaces have a higher mobility than those in the bulk of crystals. The ability of atoms to migrate on crystalline surfaces smoothes out the surface roughness to minimize the total surface energy without losing volume. Finally, the present work provides additional information on the smoothening effect of H_2 thermal annealing thanks to the spectral analysis of the roughness that shows the suppression of high- and medium-frequency roughness components after H_2 annealing.

B. Effects of Pre- and Post-Etching Treatments on the Silicon Waveguide Optical Losses

Fig. 2 shows the optical losses measured at 1310 nm and obtained after Si patterning with and without smoothening treatments as a function of the waveguide CD. The waveguide CD loss is taken into account in Fig. 2 when a smoothening treatment is introduced in the process flow.

As expected from theory, optical losses significantly increase as the CD decreases for the three patterning processes compared in Fig. 2, reflecting a strong enhancement of the interaction of the mode with sidewalls as the waveguide cross-section decreases [3]. The measurement uncertainty also becomes larger when CD decreases, due to increasing technological drifts across wafers. The BP provides acceptable optical losses ranging from 1 to 2 dB/cm for CDs larger than 500 nm. For smaller CDs, losses are dramatically larger. The introduction of the H_2 plasma smoothening treatment in the Si patterning process flow allows to reduce optical losses by 40-50% compared to the BP for all waveguide CDs. However, the losses still exceed the 1 dB/cm losses targeted. Finally, Fig. 2 clearly highlights the beneficial impact of the H_2 thermal annealing smoothening treatment on the optical losses, with a reduction by 71% for all waveguide CDs. Record optical losses below 1 dB/cm are achieved for waveguides with CDs larger than 390 nm. For 300-400-nm-wide waveguides, they range from 1.2 to 0.8 dB/cm.

Optical losses measurements at 1550 nm are also performed for the BP and the optimized process using both H_2 plasma treatment and H_2 thermal annealing. Results are compared to those at 1310 nm in Fig. 3.

For both processes, optical losses are similar above a certain waveguide CD (about 580 nm for the BP and 420 nm for the optimized process) whatever the wavelength used. For smaller waveguides, different behaviors are observed between the BP and the optimized process. Optical losses for the BP are higher at 1310 nm than 1550 nm while the trend is reversed for the optimized process. This will be discussed in section C.

C. Comparison With Payne and Lacey Theory

Fig. 4 compares the experimental and simulated optical losses at 1550 nm and 1310 nm as a function of the waveguide CDs for baseline and optimized processes. Only the experimental points relevant to the discussion have been reported on Fig. 4.

In the "high roughness" case (cf. Fig.4a), experimental data are below the theoretical curve for CDs larger than 380 nm. Indeed, it has been shown that 2D models such as Payne and Lacey's tend to overestimate scattering losses for sub-micron waveguides [16]. This suggests that for large waveguide dimensions, sidewall scattering is indeed the main cause of propagation loss. For smaller CDs, the trend is reversed and experimental losses are greater than the modeled

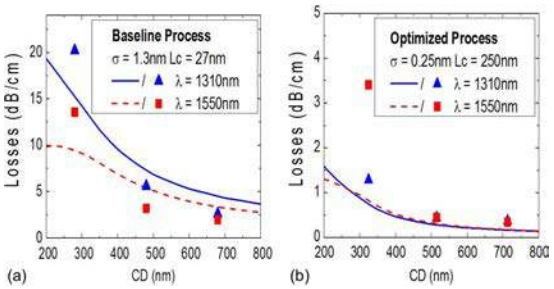

Fig. 4. Comparison between theoretical (curves) and experimental optical losses (symbols), at 1310 nm (full line) and at 1550 nm (dashed line) for: (a) the high-roughness BP and (b) the low-roughness optimized process. Symbols represent the corresponding measured losses at 1310 nm (triangles) and at 1550 nm (squares).

ones, indicating that other sources of losses contribute to the propagation loss. The most likely cause is losses induced by the lack of confinement of the mode in such high-aspect-ratio waveguide geometries, especially across the bends. Moreover, Grillot *et al*.'s [17] simulation work showed that losses due to leakage towards the substrate become not anymore negligible below a certain waveguide geometry and could largely exceed 5 dB/cm for waveguide CDs smaller than 250 nm (simulated with 1-μm-thick BOX) [17]. They showed the effect is accentuated and shifted to larger CDs as the BOX thickness decreases. However, for significant roughness, sidewall scattering – stronger at shorter wavelengths – still dominates for all CDs.

In the "low roughness" case (cf. Fig.4b), experimental losses are more important than the modeled ones for any waveguide CDs (about 0.2 dB/cm for large CDs and above 0.5 dB/cm for smaller CDs). This suggests that the losses that were neglected in the high roughness case are not anymore negligible compared to scattering losses. More specifically, Borselli *et al*. [18] found that for losses below the dB/cm level, surface absorption begins to play a significant role. Moreover, at smaller CDs, it is likely that losses induced by substrate leakage and field deconfinement across the bends are now the main contributors to the total propagation loss. As these latter sources of losses are more important at 1550 nm than those at 1310 nm, it explains why experimental losses measured at 1550 nm becomes larger than at 1310 nm at small CDs in the low roughness case.

IV. Conclusions

Minimizing scattering losses in high-index-contrast Si/SiO_2 waveguides is one of the great challenges of SOI photonic integrated chips. The primary known cause of waveguide transmission losses is scattering losses induced by sidewalls roughness. The aim of this work was to provide technological solutions to reduce the silicon waveguide sidewalls roughness during patterning in order to fabricate very-low-loss (<1 dB/cm) sub-micrometric SOI strip waveguides. To that end, H_2 plasma treatment was introduced to smooth the photoresist pattern prior to etching and H_2 thermal annealing at 850°C was applied after Si etching. These treatments have a drastic impact on the silicon sidewalls roughness, while maintaining a rectangular waveguide profile. The optimized process allows to reduce the LER down to 0.75 nm, which is almost equivalent to an atomically flat crystalline silicon surface. As a result, record-low optical losses of less than 1 dB/cm are measured at both 1310 nm 1550nm in strip waveguides with dimensions larger than 390 nm and ranged from 1.2 dB/cm to 0.8 dB/cm for 300-400-nm-wide strip waveguides. A comparison of the experimental propagation losses with a model based on Payne and Lacey equations indicates that sidewall scattering is indeed the main cause of propagation loss for undoped waveguides having sidewalls roughness of few nanometers, although, losses induced by substrate leakage and the lack of field confinement in bends become non-negligible for CDs smaller than 350 nm.

However, when the scattering losses are greatly reduced down to the dB/cm level thanks to a reduction of the waveguide sidewalls roughness below the nanometer scale, optical losses are then dominated by surface-state absorption.

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