Sub-10 nm plasma nanopatterning of InGaAs with nearly vertical and smooth sidewalls for advanced n-fin field effect transistors on silicon

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Sub-10 nm plasma nanopatterning of InGaAs with nearly vertical and smooth sidewalls for advanced n-fin field effect transistors on silicon

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This work focuses on the nanopatterning of sub-10 nm InGaAs fins by inductively coupled plasma reactive ion etching for advanced III−V n-fin field effect transistors (n-FinFETs) on silicon. First, different chlorine chemistries have been investigated and compared in order to select the most adequate one for the FinFETs process. Following this analysis, the $BCl_3/SiCl_4/Ar$ mixture was selected for the remaining of the work. Thus, a systematic study of the etching process based on this chemistry has been carried out, and the effects of the experimental conditions on the etching kinetics and the sidewalls quality have been revealed. The optimized results depict 8 nm width fins with smooth (line edge roughness ≈2 nm) and almost vertical (85° ± 1) sidewalls, opening the way for sub-10 nm width InGaAs FinFETs on silicon. © *2017 American Vacuum Society*.
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I. INTRODUCTION

For several decades, the dimensional scaling of silicon-based transistors has been the main way for increasing the performance and reducing the cost of integrated circuits. However, by pushing the miniaturization of the complementary metal-oxide semiconductor to its ultimate dimensions, the power consumption became a tremendous impediment known by the scientific community as "the power-constrained scaling limit."[1] The power consumption consisted of two parts: the static power associated with the leakage current and the dynamic power related to the switching in the transistor. Both of these two components increase drastically with the downscaling due to the rise of the short channel effects and the switching speed, respectively. The overcoming of this issue can be achieved through the introduction of innovative multigate architectures to enhance the channel electrostatic control and the integration of high-mobility materials to reduce of the supply voltage. In this context, FinFETs have emerged as a cornerstone of ultimately scaled devices. By improving the electrostatic gating, this architecture allows us to improve the subthreshold slope, to overcome the short-channel effects, and to significantly reduce the leakage currents.[2,3] Furthermore, InGaAs is establishing itself as a very promising high-mobility n-channel material for advanced scaling nodes that permits to restrict the power consumption issue by reducing the supply voltage while maintaining the current level and so the switching speed.[4–6] The integration of this material on 300 mm silicon substrates opens the way for a volume manufacturability with a fully very large scale integration compatible process flow.[7]

The InGaAs fins patterning by inductively coupled plasma reactive ion etching (ICP-RIE) is a key step of FinFETs development as it concerns the definition of the channel, the most crucial part of the transistor. So, a particular interest must be dedicated to this step, especially in the case of deeply scaled dimensions where the slightest details are critical for achieving high electrical performance. Great efforts have been invested for enhanced profile verticality,[8] sidewalls smoothness,[9] surface stoichiometry[10] and etch-induced damage mitigation.[8] Indeed, vertical-sidewall FinFETs have demonstrated better performance at low and moderately doped fins while extremely doped FinFETs are more performant when the fins sidewalls are tapered.[11,12] Furthermore, the sidewall roughness,[13] the modification of the surface stoichiometry during the etching,[12] and the ion bombardment-induced damage[14] greatly degrade the MOS interface, causing an important decline in the device reliability and electrical performance. These different aspects should be taken into account when carrying out advanced FinFETs.

Plasma etching of indium-containing III-V semiconductors has been investigated using chlorinated chemistries such as BCl_3/Cl_2,[8,15] Cl_2/N_2,[16] $Cl_2/H_2/Ar$,[17] Cl_2/Ar,[18] $SiCl_4$,[19] and $BCl_3/SiCl_4/Ar$.[14] Other gas mixtures such as CH_4/H_2 (Ref. 20) and HBr/N_2 (Ref. 21) have also been reported. However, no sub-10 nm InGaAs fins achieved by a single-step process with a vertical profile, a low surface roughness, and smooth sidewalls have been reported in the literature.

This article focuses on the characterization and development of plasma etching processes fulfilling the requirements of ultimate scaled InGaAs Fin patterning. In the first part of this work, we present the etching results of InGaAs fins with line-widths in the range of 10–50 nm using four different chlorine-based plasma chemistries in order to select the most adequate one for the fabrication of advanced III–V FinFETs. The fins' morphology has been observed by focused ion beam scanning transmission electron microscopy (FIB-STEM), and the sidewalls' roughness and the chemical composition of the surface have been analyzed, respectively, by atomic force microscopy and x-ray photoelectron spectroscopy (XPS).

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Afterward, the effects of the different experimental conditions on the etching kinetics and the quality of the sidewalls are discussed. On completion of this study, we have demonstrated 8 nm fins with smooth and nearly vertical sidewalls. These results open the way for sub-10 nm InGaAs FinFETs on silicon.

II. EXPERIMENTAL SETUP

The samples used in this study are undoped $In_{0.53}Ga_{0.47}As$ (25 nm)/InP (300 nm)/GaAs buffer (420 nm) hetero-structure, grown on a (100) orientated silicon wafer by metal organic chemical vapor deposition. The growth was performed in a 300 mm applied materials metal-organic chemical vapour deposition reactor using trimethyl-gallium and -indium as group-III precursors and tertiary butyl arsine (TBAs) and tertiary butyl phosphine (TBP) as group-V precursors.[22,23] Fins with line widths ranging from10 to 50 nm and a pitch of 200 nm are defined by e-beam lithography (JOEL6300FS system) using 60 nm of hydrogen silsesquioxane (HSQ) as an etch mask. Then, samples with an area of 1 $\times$ 1 $cm^2$are bonded to a 4-in. Si carrier wafer using PMMA to avoid the use of thermal grease that could contaminate the surface. The fins patterning is performed using an Oxford Plasma Lab 100 ICP-RIE equipment with a heated chuck and backside He cooling. A systematic study was carried out to investigate the effects of the carrier wafer, the substrate temperature, the gas flow ratios, the chamber pressure, the ICP, and radiofrequency (RF) platen powers.

After patterning, the fin profiles are characterized by scanning electron microscopy (SEM) in cross-section view using a ZEISS ULTRA$^+$ microscope in order to evaluate the fins profile as well as the etching rate. For the smallest fins with a line width inferior to 20 nm, additional observations are performed by STEM across thin lamellas prepared with FIB-STEM (Helios NanoLab 450S from FEI). The images are realized under the SEM column at 30 keV, permitting a high resolution less than 1 nm.

The sidewall line edge roughness (LER) is measured by atomic force microscopy (AFM) using a homemade setup where the sample is tilted to allow the tip to scan the sidewalls.[24] The tip of the selected AFM probe is localized at the very end of the cantilever so that it can reach the sidewall of features and has a low aspect ratio to reduce slipping issues. The images are acquired in tapping mode to reduce the sticking, and the image size is 2 $\times$ 2 μm^2.

XPS analysis of the bottom InGaAs surface is carried out immediately after the etching (few minutes) in a customized Thermo Electron Theta 300 spectrometer, using a high resolution monochromatic Al K_α source at 1486.6 eV. The detection angle was fixed at 23° referred to the normal of the wafer.

III. RESULTS AND DISCUSSION

A. Impact of wafer temperature

A first study of the etching process was performed at 20 °C using BCl_3/Ar plasma chemistry. The optimization of the gas flows, the chamber pressure and the ICP and RF platen powers allowed obtaining fins with a smooth surface. However, for any plasma conditions investigated, the fins are tapered, and the sidewall-to substrate angle is around 60° [Fig. 1(a)].

This tapered pattern profiles at a process temperature of 20 °C is attributed to the formation of $InCl_x$ thin passivation layer at the pattern sidewalls because of the low volatility of indium chloride etch byproducts at this range of temperatures.[25] The presence of the $InCl_x$ byproducts on the InGaAs surface is confirmed by the XPS analysis shown in Fig. 2(a). The increase in the process temperature from 20 to 150 °C [Fig. 2(b)] did not solve this issue. On the contrary, at 150 °C, the $GaCl_x$ and $AsCl_x$ removal rate became much faster compared to the InClx resulting in a great increase in the surface roughness. These results are in agreement with those reported by Zhao *et al.*,[14] for which the process temperature was varied between 100 and 250 °C. Thus, to balance the removal rate of In with respect to Ga and As, the process temperature was increased to 200 °C. At this temperature, the XPS peak associated with $InCl_x$ disappeared [Fig. 2(b)], and we observed a significant improvement in the profile slope (82°) and the sidewall smoothness [Fig. 1(c)]. We specify here that the plasma parameters had to be optimized at 200 °C in order to keep a fine control of the etching rate, which increases drastically with the temperature, and to prevent the degradation of the patterns. The best results were obtained with the following process conditions (using a silicon carrier wafer): BCl_3/Ar gases ratio: 15/20 SCCM, ICP power: 50 W, RF platen power: 150 W, and chamber pressure: 3 mTorr. These conditions shall be considered as a reference point for the rest of the study.

B. Chlorine chemistries comparison

In order to select the most adequate chemistry, three chlorine-based mixtures are compared on the basis of the profile slope, the bottom surface roughness, surface stoichiometry, and the etching rate for a fine control of the process. Except for the chlorine gas, the other plasma parameters are kept similar to those of the reference process mentioned above. The process time is set at 20 s for all experiments. The results are summarized in Table I.

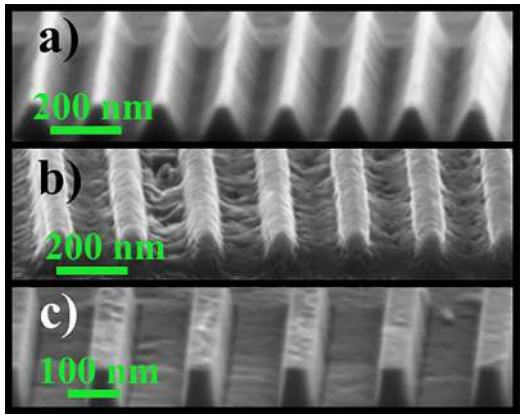

FIG. 1. (Color online) Effect of the process temperature on the sidewalls verticality: (a) 20 °C, (b) 150 °C, and (c) 200 °C.

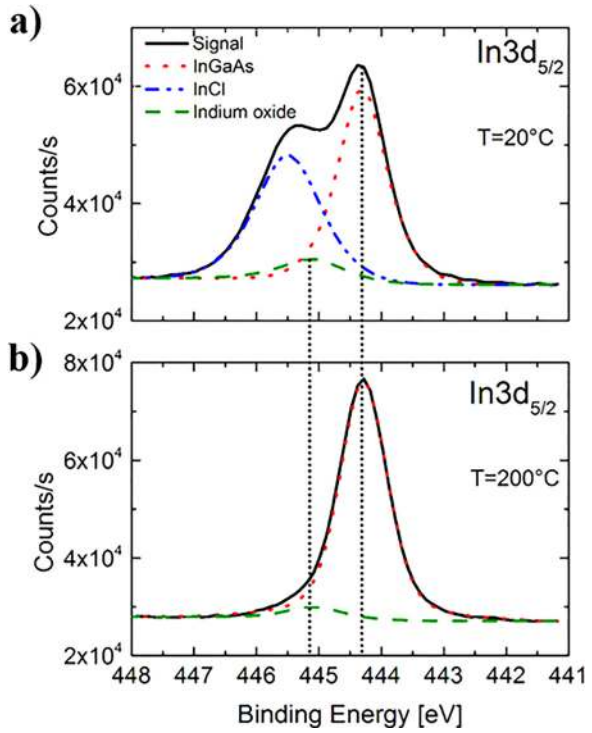

FIG. 2. (Color online) XPS spectra showing the $In3d_{5/2}$ peak of InGaAs after etching in BCl_3 based chemistry at (a) 20 °C and (b) 200 °C.

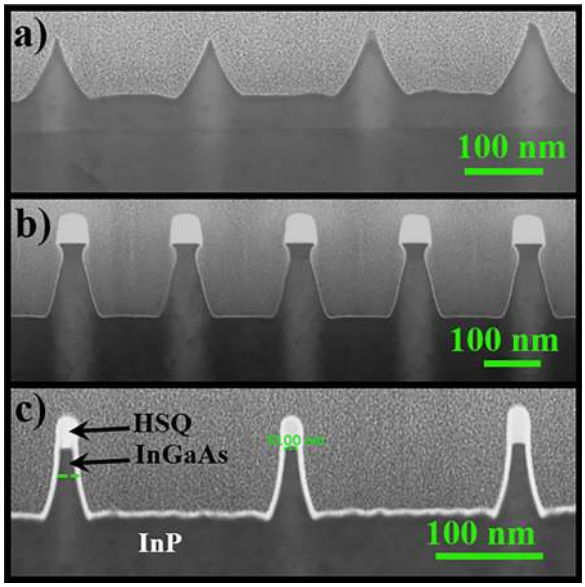

FIG. 3. (Color online) FIB-STEM images depicting the etching profiles of 10 nm wide fins obtained with three different chlorine plasma chemistries: (a) Cl_2/Ar, (b) $SiCl_4$/Ar, and (c) BCl_3/Ar.

As illustrated in Fig. 3(a) and Table I, the etch rate of the Cl_2-based chemistry is much higher than the other two chemistries. Moreover, the InGaAs/SiO_2 etch selectivity is very poor and after 20 s of plasma process, the etching mask is totally consumed, which results in degraded profiles. Indeed, by operating at 200 °C, the desorption of $InCl_x$ compounds is not anymore the limiting step, and the etching kinetics are rather driven by the supply of etching species, mainly atomic chlorine. It is suspected that in Cl_2 based plasma, the atomic chlorine density is higher because of the twice lower bond dissociation energies of Cl_2 (242.5 kJ/mol),[26] compared to Si-Cl (456 kJ/mol)[26] and B-Cl (536 kJ/mol).[26] Even after reducing the Cl_2 flow from 15 to 5 SCCM and the ICP power from 50 to 20 W, the etch rate of Cl_2/Ar remained too high (≈11 nm/s) for a fine control of the process at 200 °C and this plasma chemistry has been abandoned.

On the other hand, the $SiCl_4$/Ar chemistry is much less aggressive than Cl_2/Ar. However, the etching rate still remains too high compared to BCl_3/Ar. AFM analyses of the etched surface shows that the surface roughness (RMS) is almost similar to the one before plasma exposure for BCl_3 and slightly increased for $SiCl_4$ plasma. In addition to this, a clear undercut have been observed in the case of $SiCl_4$/Ar chemistry [Fig. 3(b)] due to its low anisotropy at low ion density.[19]

The XPS analyses of the InGaAs surface composition after exposure to $SiCl_4$/Ar and BCl_3/Ar plasmas (see Fig. 4 and Table I) show a great similarity between the two surfaces. Both are As rich (≈60%), which was already observed in the case of InGaAs chlorine etching[12] and could lead in some case to surface Fermi-level pining.[27] However, it is important to mention that the analyzed surface here is the postetch bottom surface. A more rigorous study requires analyzing the sidewalls composition that could be slightly different from the postetch bottom surface. This depends on the degree of the etch anisotropy as for an anisotropic etch process the bottom surface is exposed to more ion bombardment while the sidewalls could see deposition of plasma species and etch byproducts.[12]

The FIB-STEM observation and the AFM analysis of the surface show that BCl_3/Ar mixture [Fig. 3(c)] seems to be the most adequate as it provides near vertical sidewalls (82°), the lowest etch rate (2.6 nm/s) and the lowest surface roughness (RMS = 0.83 nm) among the three chemistries. To further improve the sidewall slope, a few SCCM of $SiCl_4$ were introduced to the plasma as reported by Zhao *et al.*[9] After optimization, the best results were obtained with 15

TABLE I. Comparison of the etching results obtained with the three chlorine-based chemistries.

Chlorine chemistry	Morphology	Etching rate (nm/s)	Surface RMS (AFM 5 × 5 μm)	Surface composition (XPS)
Before etching	***	***	0.79 nm	In:28% Ga:26% As:46%
Cl_2/Ar (15:20)	Damaged patterns	15	***	***
$SiCl_4$/Ar (15:20)	Important undercut	7.2	0.95 nm	In:21% Ga:18% As:61%
BCl_3/Ar (15:20)	Nearly vertical sidewalls	2.6	0.83 nm	In:20% Ga:18% As:62%

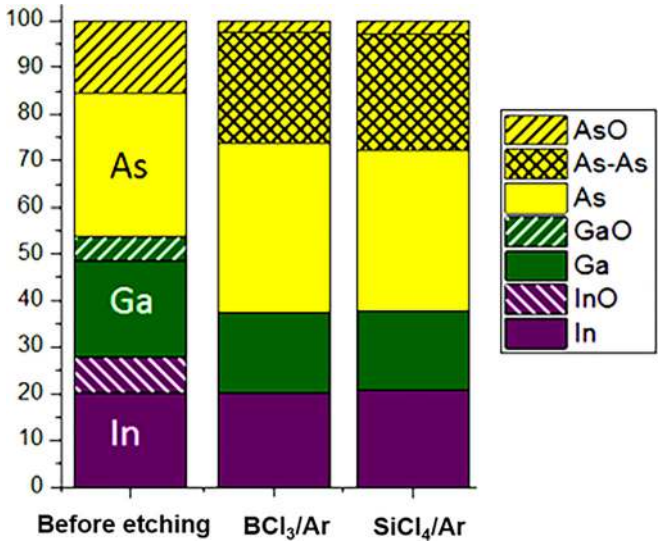

FIG. 4. (Color online) XPS analysis showing the evolution of chemical composition of the InGaAs surface after exposure to BCl_3/Ar and $SiCl_4$/Ar plasmas.

SCCM of BCl_3, 5 SCCM of $SiCl_4$, and 20 SCCM of Ar [Fig. 5(a)]. For these conditions, a low etch rate of about 2.5 nm/s and a high sidewall slope of 85° are measured.

C. Impact of etching conditions

In the next set of experiments, the process temperature (200 °C) and the $BCl_3/SiCl_4$/Ar chemistry have been retained while the remaining RIE experimental conditions are varied and compared to the reference point described above.

First, the impact of the carrier wafer has been studied. The SEM images [Figs. 5(a) and 5(b)] corresponding to the InGaAs fin patterning using the $BCl_3/SiCl_4$ reference process with Si and SiO_2 carrier wafer, respectively, show similar pattern profile and sidewall angle (around 85° ± 1). However, the etch rate decreases sharply from 4.8 to 2.5 nm/s with the use of a silicon wafer [Fig. 5(a)]. This is explained by the loading effect. Indeed, conversely to the inert SiO_2 surface, a portion of the reactive chlorine species react with the silicon surface, which represents 98.7% of the total surface and are not anymore available to etch the InGaAs sample, involving a drop of the InGaAs etching rate.

Furthermore, the increase in the Ar flow at the expense of BCl_3 [Fig. 5(c)] induces a rise in the etching rate of ≈70% due to increased ion sputtering. Indeed, in the case of a high RF platen power and a low ICP power such as our process (RF platen power: 150 W and ICP power: 50 W, bias voltage: −455 V), the physical etching due to the ion bombardment is predominant. Ar is heavier than B, Cl, and Si and its increase enhances the physical etching. On the other hand, there is no significant effect of the Ar flow increase on the sidewall slope and roughness. The effect of ICP power was also studied [Fig. 5(d)]. We have observed that when the ICP power increases from 50 to 100 W, the sidewall slope is improved and becomes quasivertical in the InGaAs part of the fins. However, the etching rate became too high (7.2 nm/s) for a fine control of the process.

The increase in the chamber pressure causes an undercut and a decrease in the etching rate. In fact, it reduces the mean path of the reactive species, and so, it promotes the ion collisions and the isotropic etching.[28] The decrease in the etching rate, compared to the reference sample, could be explained by a less directional ion bombardment due to the enhanced ion collisions under higher chamber pressure.[29]

This analysis shows that the reference conditions present a very good compromise allowing the definition fins with a high profile slope (85°), a low etching rate (2.5 nm/s), and smooth sidewalls.

D. Sub-10 nm fins with smooth and nearly vertical sidewalls

Thanks to a fine control of the e-beam lithography and the optimization of etching process, as detailed in the previous paragraph, we demonstrate 8 nm fins with quasivertical [Fig. 6(a)] and smooth sidewalls [Fig. 6(b)]. The sidewall line edge roughness (LER) has been measured using tilting AFM probe (described above in part II). This roughness is mainly due to the transfer of the HSQ mask roughness associated with the lithographic process, which is initially around 4.5 nm (the continuous line). During etching, this roughness was smoothed out to reach a value of approximately 2.5 nm at the bottom part of the HSQ mask and, respectively, 2.2 and 2 nm at the InGaAs and InP sidewalls (dashed line).

The sidewalls roughness as well as the fins width could be further reduced through a digital etch cycle based on a self-limited oxygen plasma oxidation followed by a diluted H_2SO_4 rinse for oxide removal, as reported in different studies.[8,14,28]

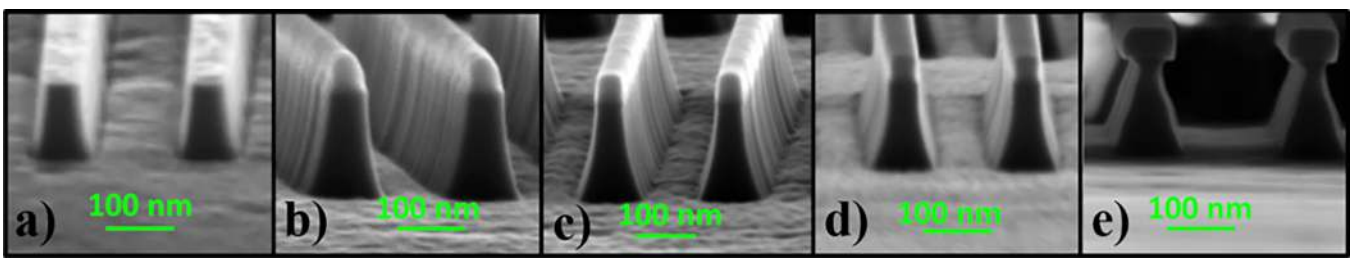

FIG. 5. (Color online) InGaAs fins obtained under different experimental conditions: (a) optimum process (ref.) $BCl_3/SiCl_4$/Ar flow ratio = 15/5/20 SCCM), (b) carrier wafer: SiO_2 (vs Si), (c) $BCl_3/SiCl_4$/Ar flow ratio = 10/5/25 SCCM (vs 15/5/20 SCCM), (d) ICP power = 100 W (vs 50 W), and (e) RF platen power = 50 W (vs 150 W).

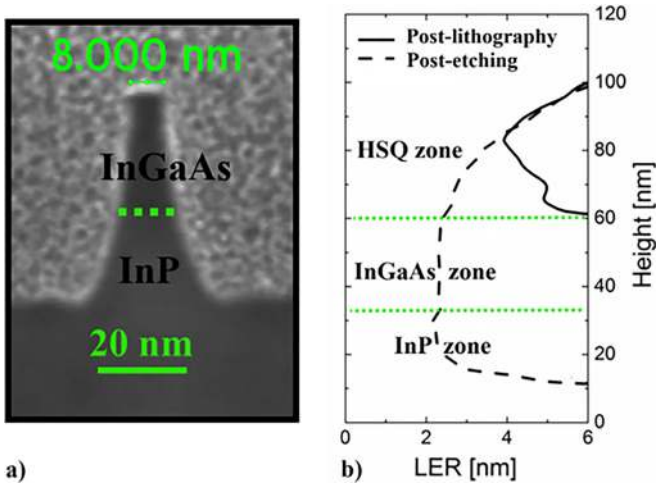

FIG. 6. (Color online) (a) FIB-STEM view of a 8 nm InGaAs fin realized using $BCl_3/SiCl_4$ etch process (b) analysis by tilting AFM of the sidewall line edge roughness of the initial HSQ mask (dashed line) and the InGaAs/InP etched fins (continuous line).

IV. CONCLUSIONS

Sub-10 nm $In_{0.53}Ga_{0.47}As$ fins integrated on silicon with a quasivertical profile (sidewall to substrate angle = 85°) and smooth sidewalls (LER ≈ 2 nm) have been demonstrated using $BCl_3/SiCl_4/Ar$ plasma process. A systematic experimental study was carried out and allowed to reveal the impact of the different plasma parameters and identify the optimal conditions for the high resolution fins patterning. The postetch InGaAs surface was analyzed by AFM and XPS. It presents a low RMS roughness of 0.8 nm and seems to be As rich (≈60%). It is expected that sidewalls surface more sensitive to the chemical etching are also enriched in As. Further improvement is needed to ameliorate the surface stoichiometry. These results are very promising for the realization of advanced III–V n-FinFETs on silicon.

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