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ABSTRACT

We report a 20 nm half-pitch self-aligned double patterning (SADP) process based on a resist-core approach. Line/space 20/20 nm features in silicon are successfully obtained with $CD_{variation}$, LWR and LER of 0.7 nm, 2.4 nm and 2.3 nm respectively. The LWR and LER are characterized at each technological step of the process using a power spectral density fitting method, which allows a spectral analysis of the roughness and the determination of unbiased roughness values. Although the SADP concept generates two asymmetric populations of lines, the final LWR and LER are similar. We show that this SADP process allows to decrease significantly the LWR and the LER of about 62% and 48% compared to the initial photoresist patterns. This study also demonstrates that SADP is a very powerful concept to decrease CD uniformity and LWR especially in its low-frequency components to reach sub-20 nm node requirements. However, LER low-frequency components are still high and remain a key issue to address for an optimized integration.

Keywords: SADP, LER, LWR, spectral analysis, PSD, CD-SEM

1. INTRODUCTION

Double patterning techniques have emerged as the mainstream solution to overcome 193 nm photolithography resolution limits, while waiting for the next generation lithography such as EUV, DSA, nanoimprint or multi-ebeam lithography [1-11]. They are now widely implemented in the manufacturing of memory and logic devices. Among all the double patterning techniques available, self-aligned double patterning (SADP) approach is a promising candidates for the sub-20 nm technological nodes. It combines subsequent lithography, deposition and plasma etching steps to halve the pitch defined by state-of-the art 193 nm immersion lithography. Principle of this technique is quite simple and is described in Figure 1. A spacer material is deposited uniformly on pre-patterned features called the core or mandrel. Then, the spacer material is etched back and the core is removed, leaving the spacer on the core sidewalls. Finally, the spacer patterns, whose density has been doubled compared to the initial features serve as an etching mask. Using this approach, the pitch can be divided indefinitely with a succession of spacer formation and pattern transfer processes. Aggressive dimensions targeted sub-20 nm nodes could thus be achieved.

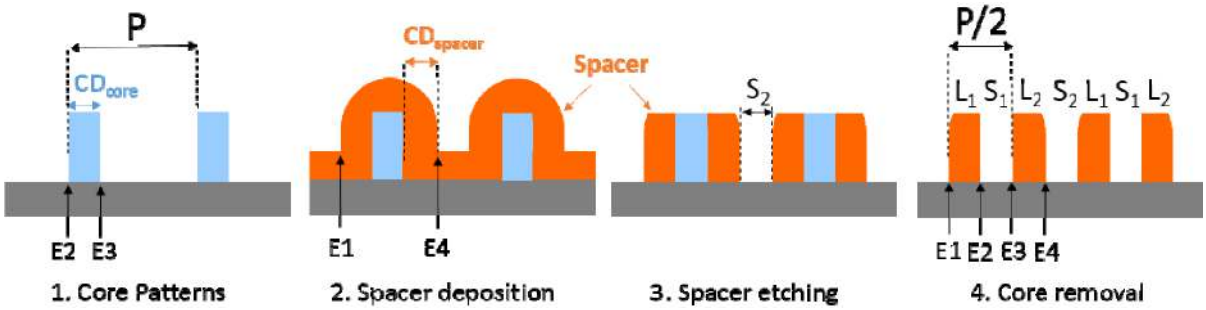

Figure 1: Schematic of the self-aligned double patterning technique.

The SADP technique has been extensively reported as an efficient strategy to print very fine, uniform and dense features [6,8,11]. However, less studies have investigated in details its capability in term of sidewall roughness [9-11]. Sidewall roughness is today a critical issue that limits CMOS downscaling since it degrades device electrical performances. It can

be described by two main parameters: the line width roughness (LWR), which is the variation of the critical dimension (CD) of a line along its length and the line edge roughness (LER), which is the variation of the edge roughness amplitude along the line. For the sub-20 nm technological nodes, LWR and LER must be controlled at less than 2 nm while best optical lithographies allow to achieve patterns of 4-5nm LWR. Understanding and minimizing line roughness at this nanometer scale thus requires an accurate and insightful characterization of the sidewall roughness.

In this work, we have developed a 20 nm half-pitch SADP process flow using 40 nm half-pitch resist patterns as the core materials, and to characterize finely the LWR/LER evolution at each technological steps. A power spectral density (PSD) fitting method is used to provide a spectral analysis of the roughness and the determination of unbiased roughness values. Motivation for this study is that the SADP concept leads to 2 asymmetric populations of lines L_1 and L_2 and 4 populations of edges E_1, E_2, E_3 and E_4 (Figure 1), which could have different roughness behavior and impact the final lines. Indeed, two of them, E_2 and E_3 originate from the line edge of the core material, while E_1 and E_4 originate from spacer deposition.

2. EXPERIMENTAL SET-UP

This SADP process using a resist-core approach consists in depositing a spacer film directly on resist patterns printed by lithography. This integration presents several benefits compared to the conventional hard mask approach, since it uses a simplified stack and requires less technological steps, leading to an improved cost of ownership. The next paragraphs describe the tools and characterization techniques involved in this process.

2.1 Lithography

E-beam lithography is used to define resist patterns with a pitch of 80 nm on a stack made of 30 nm-thick Silicium Antireflective Coating (SiARC), 70 nm-thick Spin On Carbon layer (SOC) and 300 mm diameter Si wafer. The e-beam lithography tool (SB3054 from VISTEC) is a single variable shaped electron beam exposure tool using a LaB6 source and an acceleration voltage of 50kV. With a dose of 8.6 $\mu C/cm^2$, patterns with critical dimensions of about 40 nm, and height of 50 nm are printed in the positive chemically amplified resist, CAP64 from TOK.

2.2 Deposition tool

SiO_2 film are deposited on the photoresist patterns using Plasma Enhanced Atomic Layer Deposition (PEALD) technique in an EmerALD tool from ASM. Key advantages of this technique are highly conformal and uniform films. A low deposition temperature of 50°C is used to prevent resist degradation. The deposition process alternates cycles of injection of bis(diethylamino) silane BDEAS (SAM 24) as silicon precursor followed by O_2 plasma. The growth per cycle (GPC) is ~0.135 nm/cycle at 50 °C. Thickness uniformity is less than 0.4 % in 1 sigma (49 points measured by ellipsometry). The thickness deposited on the resist patterns is tuned by the deposition process time.

2.3 Plasma etching tool

The plasma etching processes are developed in an inductively coupled plasma (ICP) source, DPS from Applied Materials. The DPS is a high density plasma source where both the source antenna and the bottom electrode are powered. The reactor chamber walls are coated with Al_2O_3. The plasma is excited inductively via two RF coils (13.56 MHz) to improve the ion flux uniformity. The chuck temperature is kept at 55°C, the chamber walls are kept at 60°C and the ceramic dome is maintained at 65°C. To ensure a good reproducibility, the chamber walls are cleaned in SF_6/O_2 plasma before each experiment.

2.4 Process characterization

2.4.1 Pattern profiles

Patterns profiles are characterized at each technological step involved in the SADP process flow using SEM cross sections observations performed in a HITACHI S5000.

2.4.2 CD control and LWR/LER

CD-SEM technique is used to characterize the critical dimension (CD), and the sidewalls roughness (LWR and LER) of the lines after each technological step involved in the SADP integration. Top view SEM images are captured with a Hitachi CG4000 using a rectangular scanning mode and a 1024*1024 pixel definition. This mode allows different magnifications along the x and y axis, 300000 and 49000 respectively in our case, which is very convenient to get a high

resolution along the x axis while analyzing a significant section of the line along the y axis. The pixel size is 2.69 nm and 0.44 nm along the y and x axis respectively. The accelerating voltage is 300 V if resist patterns are under observation and 500 V otherwise.
SEM images are then analyzed off-line using Terminal PC software from Hitachi. In agreement with another study [13], our choice is to average 25 pixels across the resist line (smoothing parameter), 7 pixels otherwise. Three other parameters are available on the Terminal PC software and have an impact on sidewall roughness values: the inspect area, IA (or the measurement line length), the measurement points, N and the sum line, S (or averaging pixel along the y axis). The values chosen are IA=800 pixels corresponding to a line length of L=2152 nm, S=2 and N=400.
It is known that metrology tools introduce some noise and cause errors in roughness measurement. The edge detection of CD-SEM images include some noise, which is white and uncorrelated to the "real" roughness [12]-[15]. It can been described as follow:

$$\sigma_0^2 = \sigma_{\text{real}}^2 + \sigma_{\text{noise}}^2 \quad (1)$$

where, σ_0^2 is the variance of the edge positions as measured by the metrology tool, σ_{real}^2 is the variance of the "real" edge positions and σ_{noise}^2 is the variance of the random noise. To extract the noise level, a method has been recently developed [16], based on the PSD fitting method proposed by Hiraiwa and al. [13-14]. It consists in acquiring a large set of CD-SEM images of lines (N*) in order to calculate a power spectral density (PSD) of the LWR and LER. The final PSD is the average of the N* calculated PSD and is then adjusted with an analytical function. In this study, we choose N*>200 to have better statistics and smooth the PSD. The analytical function used to fit the experimental data is composed of three components (Equation (2)). The two first components described the self-affine fractal behavior of the roughness to take into account its low frequency distribution and the third one represents the white noise level of the equipment.

$$P_n = \frac{\Delta y}{2\pi N}\sigma_{real1}^2\left[\sum_{m=-N+1}^{N-1} e^{-\left|\frac{m\Delta y}{\xi_1}\right|^{2\alpha_1}} e^{-ik_n m\Delta y}(N-|m|)\right] + \frac{\Delta y}{2\pi N}\sigma_{real2}^2\left[\sum_{m=-N+1}^{N-1} e^{-\left|\frac{m\Delta y}{\xi_2}\right|^{2\alpha_2}} e^{-ik_n m\Delta y}(N-|m|)\right] + \frac{\Delta y}{2\pi}\sigma_{noise}^2 \quad (2)$$

For each two first components, the roughness is described by three parameters:

-the roughness amplitude, σ_{real1} and σ_{real2}

-the correlation length, ξ_1 and ξ_2, that represents the distance beyond which edge points can be considered uncorrelated

-the roughness exponent, α_1.and α_2, which varies between 0 and 1 and gives the relative contribution of high frequency fluctuations to LER or LWR. Large values of α indicate less high frequency fluctuations.

In equation (2), Δy is the measurement interval, i.e. L/N=2152/400 in our case.
Finally, the real LER (or LWR) is given by equation (3):

$$LER_{real} = 3 * \sqrt{\sigma_{real}^2} = 3 * \sqrt{\sigma_{real\,1}^2 + \sigma_{real\,2}^2} \quad (3)$$

More details on the proposed PSD fitting method and its efficiency to extract the measurement noise ($3\sigma_{noise}$), and the unbiased roughness parameters ($3\sigma_{real}$, ξ and α) can be found in reference [16].

3. EXPERIMENTAL RESULTS

3.1 SADP process flow

Figure 2 describes all the technological steps involved in our SADP process flow with the corresponding top view CD-SEM and cross-sectional SEM images. Figure 3 summarizes the CDs of the lines and its CD variation extracted from the CD-SEM images at each steps.

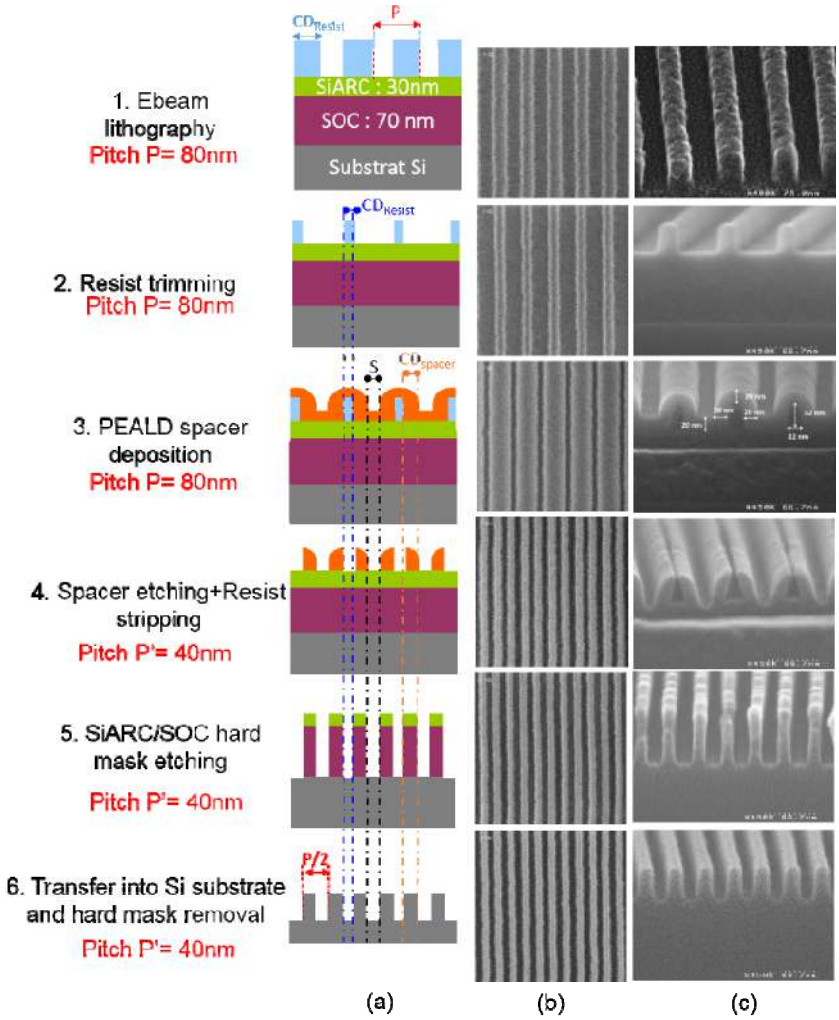

Figure 2: Technological steps involved in the resist-core SADP integration: (a) schematic diagram, (b) top-view CD-SEM images, (c) cross-section SEM images.

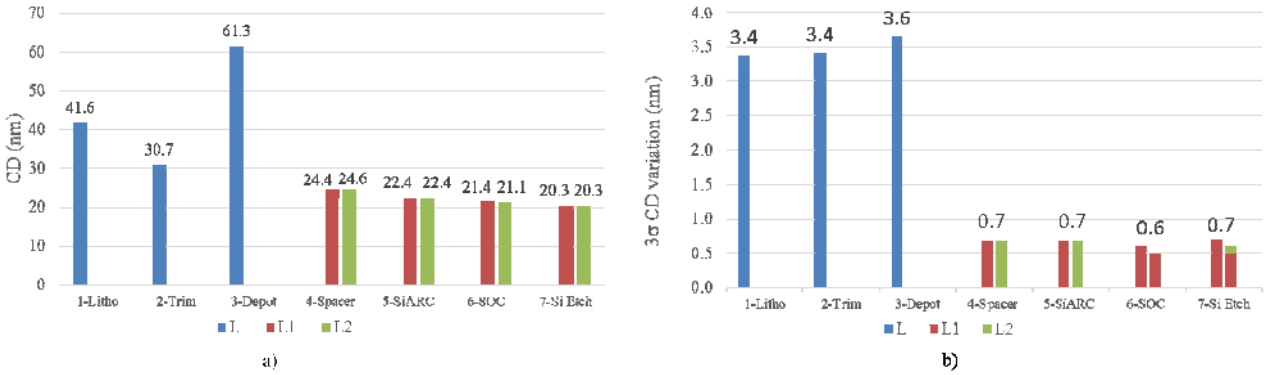

Figure 3: CD-SEM measurements performed after each technological step involved in the SADP process: (a) Critical dimensions of the lines, (b) 3σ CD variation.

In a SADP process, to get regular line-space patterns after the pitch division, two key parameters must be carefully controlled:

- CD_{spacer}, the spacer thickness deposited on the core sidewalls. It defines CDs of the final lines L_1 and L_2.
- $CD_{core,}$ the CD of the core patterns that will define the space S_1, In our case, the core is made of resist as referred on Figure 1 and Figure 2.

As the pitch P is constant and equal to P= L1+L2+S1+S2, then the space S_2 is naturally adjusted if CD_{Resist} and CD_{spacer} are well controlled.

While CD_{spacer} is easily tuned by the deposition process duration, CD_{Resist} can be adjusted by introducing a plasma etching step, called resist trimming before the deposition step. This plasma step was introduced in the early 2000's to overcome optical lithography resolution limit and to reach the appropriate critical dimension required at each technology node. This particular plasma step typically uses O_2-based plasma chemistry in order to achieve an isotropic etching of the resist pattern and induce a controlled lateral erosion of its critical dimension [17-19]. If trimming processes can decrease the resist dimensions, they cannot increase the pattern density. The reduction in resist linewidth is also accompanied by a corresponding increase in space between lines, thereby preserving the original pitch defined by the lithography. In this study, a HBr/O_2 plasma process with no bias power applied to the substrate is developed and leads to -0.7 nm/s lateral etch rate. By adjusting properly the resist trimming step, the resist CD can be finely tuned.

Preliminary studies have shown that to get regular 20/20 nm line/space features in silicon, CD_{Resist} must be about 30 nm prior deposition and the thickness deposited on the resist core sidewalls, CD_{spacer} should be of 20 nm. Starting from resist CDs of about 40 nm after lithography, the HBr/O_2 plasma etching time is adjusted to target a resist CD of 30 nm. After the deposition step, SEM cross-sections observations of Figure 2c confirm a 20 nm-thick conformal SiO_2 spacer material deposited on the resist pattern. The resist patterns profile are preserved during the deposition step, confirming that this low temperature deposition step is indeed compatible with the low thermal resist budget. However, SEM cross-sections of Figure 2c and CD-SEM measurements of Figure 3a show that there is a 9.4 nm resist CD loss during the deposition step. This is not surprising since the PEALD process involves one cycle of oxygen plasma that is known to lead to resist trimming. This lateral erosion occurs during the first cycles of the PEALD process, when the SiO_2 layer is not thick enough to prevent from the diffusion of oxygen radicals down to the resist. After a CF_4 plasma process dedicated to the etching of the SiO_2 spacer material followed by an O_2 plasma step aimed to remove the resist core materials, two populations of line are generated with similar CD of about 24.5 nm. The patterns CD are decreased down to 22.4 and 21.1 nm during Si ARC etching in CHF_3/CF_4/Ar plasma and SOC etching in HBr/O_2 respectively. Finally, after silicon etching in SF_6/CHF_3/Ar plasma and SOC hardmask removal in O_2 plasma, regular line equal space 20/20nm silicon patterns are obtained. Figure 3b shows the critical dimension variation measured over 200 line segments in the same dye after each technological steps involved in the SADP process. It is observed that the $CD_{variation}$ is very high after the e-beam lithography step, of about 3.5nm and that this significant value is transferred during both the resist trimming and deposition steps. However, once the two population of lines are generated after the spacer etching step, the $CD_{variation}$ of both lines are very low, of 0.7 nm, reaching thus the ITRS specifications in terms of CD control.

This first section demonstrates the potential of a resist-core SADP process to achieve line equal space 20/20 nm silicon features with a $CD_{variation}$ below 1 nm, starting with an 80 nm pitch lithography.

3.2 LWR/LER evolution

Using the protocol described section 2.4.2, real roughness values for LWR and LER have been determined and spectral analyses have been performed after each technological step of the SADP process as shown in Figure 4 and 5 respectively. Concerning the LER, LER_{left} and LER_{right} are measured for each population of lines present after each technological step. Thus, after the lithography and resist trimming step, LER_2 and LER_3 correspond to LER_{left} and LER_{right} of the resist patterns, respectively. After the deposition step, LER_1 and LER_4 correspond to the LER_{left} and LER_{right} of the spacer deposition. After spacer etching and core removal, two asymmetric populations of lines L_1 and L_2 are generated with LER_{left} and LER_{right} originating from different technological step. LER_1 and LER_2 are the LER_{left} and LER_{right} of L_1, while LER_3 and LER_4 are the LER_{left} and LER_{right} of L_2.
After the lithography step, the resist LWR and LER are quite significant of 6.3 nm and 4.4 nm, respectively. Similar trend is observed for both LWR and LER after the resist trimming and the deposition steps. The LWR and LER are decreased of about 20% after the resist trimming step, resulting in a 3.8 nm LWR and 3.3 nm LER. Figure 4(b) and 5(b) show that the roughness reduction occurs in the high-frequency roughness range. This trend has already been observed for 193 nm photoresist patterns exposed to HBr and HBr/O_2 plasma treatment [20-22]. It can be explained by the simultaneous actions of the VUV plasma emission and the chemical etching of the atomic oxygen present in O_2 based

plasma. The VUV flux can chemically modified the bulk of the photoresist patterns and leads to the outgassing of photoetching byproducts, which is followed by polymer chain rearrangement and leads to resist smoothening [20-21]. The isotropic etching of atomic oxygen can remove preferentially all the protuberances present on the resist sidewalls and also results in a surface roughness reduction [22]. After deposition, there is also a 20% decrease for both LWR and LER, also occurring in the high-medium frequency range. This can also be explained by the fact that during the deposition process, the resist pattern is laterally eroded by the atomic oxygen present during the O_2 plasma cycle, and as previously explained, it can leads to resist smoothening. As the SiO_2 spacer deposition is conformal, it replicates the resist pattern profile and roughness that is smoothed during the deposition process. Thus, although it cannot be confirmed experimentally, we suspect that LER_2 and LER_3 are smoothed during the deposition process resulting in reduced LER_1 and LER_4

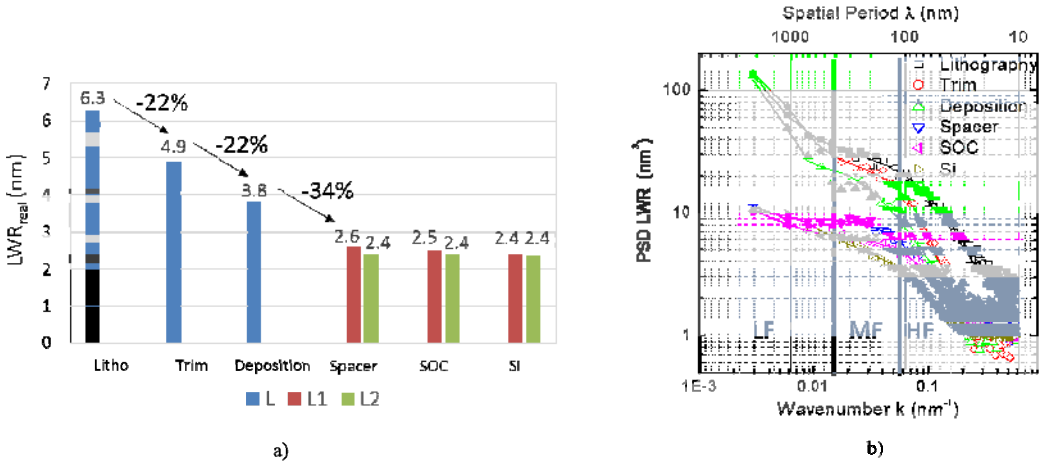

Figure 4: (a) LWR_{real} extracted from the CD-SEM image analyses and the PSD fitting procedure, and (b) Power spectral density (PSD) of the LWR, after each technological step involved in the SADP. After noise removal, PSDs are arbitrarily shifted to 1 for log scale plotting.

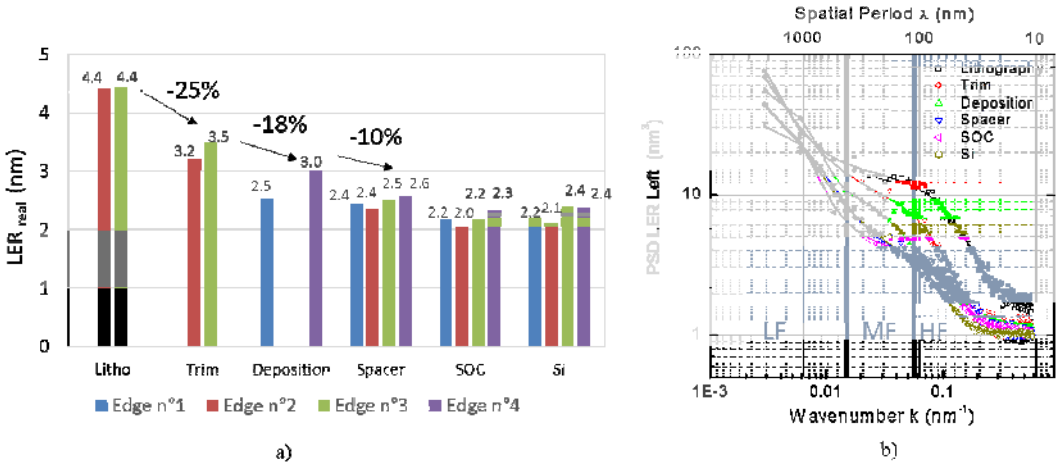

Figure 5: (a) LER_{real} extracted from the CD-SEM image analyses and the PSD fitting procedure, and (b) Power spectral density (PSD) of the LER, after each technological step involved in the SADP. After noise removal, PSDs are arbitrarily shifted to 1 for log scale plotting.

It should be mentioned that most of the time, the LER_{right} is higher than the LER_{left}. We suspect that this trend is not real and comes from a measurement artefact. Indeed, the e-beam of the CD-SEM scans the wafer with an angle slightly off

the normal. Consequently, the electron-resist interaction is slightly different for the left and right edges, resulting in different image contrast and different noise level for the two edges. Although the PSD fitting procedure that we use allows to extract the equipment noise level which is usually higher for right edges than for left edges, we do observe a shift between LER_{left} and LER_{right} that we cannot explain.

After the spacer etching step and core removal, the behaviors of LWR and LER are different. Concerning the LWR, it is observed a significant decrease of 34% occurring mainly in the low-frequency range of roughness. The two populations of line have similar LWR of about 2.5 nm, which is subsequently transferred during the SiARC/SOC hard mask and silicon plasma etching steps (Figure 4(a)). Regarding the LER, the roughness decrease is much less pronounced (of only 10%) because the low-frequency roughness components are much less impacted by the process. A slight LER improvement is however noticed during the hard mask and silicon etching steps, resulting in a final LER of about 2.3 nm. It can also be noted that the four populations of LER values are quite similar. It could have been expected that LER_2 and LER_3 might be more important than LER_1 and LER_4, since LER_2 and LER_3 originate from resist sidewalls roughness that is measured of 3.3 nm after the resist trimming step, whereas LER_1 and LER_4 originates from the spacer deposition sidewalls roughness measured of about 2.7 nm. The fact that the four LERs are quite similar after spacer etching reinforces the assumption made previously that LER_2 and LER_3 are reduced during the deposition process, and that LER_1 and LER_4 replicates the LER_2 and LER_3 smoothed during the deposition.
The significant decrease of LWR in the low-frequency range can be easily explained by the highly conformal deposition, as schematically represented in Figure 6. Indeed, a conformal deposition implies that the thickness deposited on the resist core is constant all along the resist line length, that is to say that the CD of the two populations of lines L1 and L2, the so-called CD_{spacer}, should be constant all along the line length. It means that the LWR of L1 and L2, which is, by definition, the standard deviation of CD_{spacer}, should be theoretically of zero. In our case, although the SADP concept allows to decrease significantly some of the low frequency roughness, a 2.4 nm LWR is still remaining because either the deposition process is not 100% conformal or because the plasma etching steps that have been developed introduced some roughness. Concerning the LER, Figure 6 tries to schematically explain why the conformal deposition will not have a benefic impact on the low frequency roughness components, like for the LWR. As the deposition replicates the resist sidewalls, if some low-frequency roughness components are present after the lithography and resist trimming steps, those will be further transferred to the spacer sidewalls, while in the case of LWR, the conformal deposition erases them. Those low-frequency roughness components are usually generated during the lithography step, and are extremely difficult to be removed during either a resist plasma treatment or plasma etching transfer, that generally show a roughness reduction in the high/medium frequency range [24]. References [22, 25] showed a beneficial impact of thermal treatment on photoresist pattern linewidth/line edge roughness in the low-frequency region, although the roughness reduction is not as significant as for the SADP concept. Moreover, the bake process window is very limited, and the obtained roughness improvement is photoresist chemical platform-dependent. Indeed, not adapted bake conditions could lead to resist reflowing.

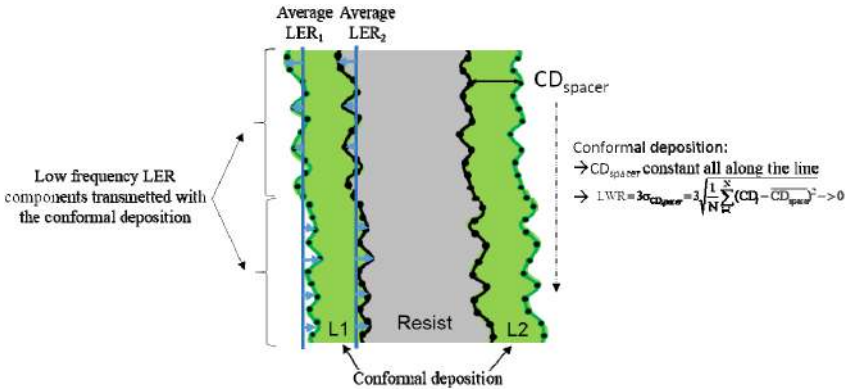

Figure 6: Schematic illustrating the impact of a conformal deposition on the decrease of low-frequency LWR components.

Another point that has to be pointed out is that in the present study, e-beam lithography using a shaped beam exposure tool has been used to print the photoresist patterns. This technique leads to "shot butting" defects (illustrated in Figure 7) that correspond to a misalignment of few nanometers of the square boxes (X (up to1.6µm)*Y= 1.25µm) used to write

patterns. This defect introduces significant low-frequency roughness components, which partially explain the significant LWR and LER after lithography of this study [26]. Such phenomenon may also reduce the beneficial impact of the conformal deposition to reduce low-frequency roughness components, explaining why the final LWR/LER values are not so decreased compared to other studies using optical lithography [9-11].

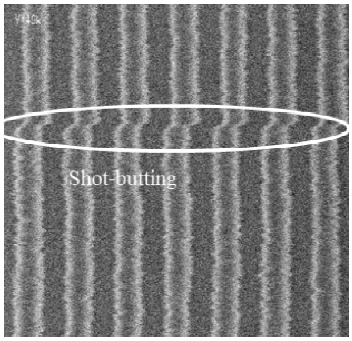

Figure 7: Illustration of shot-butting defects occurring with shaped ebeam exposure tools.

4. CONCLUSION

In this study, we have demonstrated a successful integration of a resist-core self-aligned double patterning process to achieve 20/20 nm silicon features with $CD_{variation}$, LWR and LER of 0.7 nm, 2.4 nm and 2.3 nm respectively. The spectral analysis of the LWR has shown that the high-frequency components of the LWR are decreased during the resist trimming and deposition steps due to the smoothening effect of O_2-based plasma on resist. LWR low-frequency components are significantly reduced after the spacer etching step when the two populations of line are created. This phenomenon is attributed to the high conformity of the spacer deposition with the PEALD technique. The LERs are also significantly decreased during the trimming and deposition steps in the high-frequency domain, but the beneficial impact of the highly conformal spacer deposition on low-frequency roughness components is not as important for the LER than for the LWR. Consequently, the whole SADP process flow developed in our study can lead up to a 62% LWR decrease against only a 48% LER decrease, compared to the initial photoresist patterns. It should be mentioned that the reduction of the LWR and LER during the deposition step occurs because the O_2 plasma used in the deposition process smoothens the resist. The use of another couple of core material and spacer material could result completely different results. The present study has also shown that although the SADP concept generates two asymmetric populations of lines, the latter have similar LWR, and similar left and right LER. The final silicon lines LWR and LER values of 2.4 nm and 2.3 nm could certainly be improved further by starting with more optimized lithography. Indeed, the e-beam shaped exposure tool used in this study, is less suitable than optical lithography to print photoresist patterns with low LWR and LER, especially in the low-frequency range because of the shot-butting defects. Moreover, combining optical lithography with optimized resist cure plasma treatment could help in decreasing further the photoresist LWR and LER and, subsequently the LWR and LER of silicon patterns. This study has demonstrated that SADP is a very powerful concept to decrease CD uniformity and low-frequency LWR components. Using such approach, the ITRS specifications in terms of LWR and CDU for the sub-20 nm technological node could be reached. However, even with the SADP approach, the low-frequency LER components still constitute a key issue for the advanced nodes.

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